

COURSE PLAN AND EVALUATION PLAN

- | | | | |
|------------------------------|--------------------------|-------------------------|--|
| 1. Course Code: | EC300 | 2. Course Title: | DIGITAL SYSTEM DESIGN |
| 3. L – T – P: | 3-1-0 | 4. Credits: | 4 |
| 5. Pre-requisite: | EC202 | 6. Teaching Department: | Electronics & Communication Engg. |
| 7. Course Instructor: | Dr SUMAM DAVID S. | | |
| 8. Objectives of the Course: | | | |

At the end of the program the student must be able to

Design digital systems using VHDL, given a set of specifications
 Implement digital systems using Programmable ASICs (Xilinx FPGAs)

9. Course Coverage (40 – Lecture Schedule) :

Module	Contents	Objectives	Lecture	Evaluation
Introduction	Introduction to DSD – Objectives of the course, motivation, course plan, evaluation method, references	<ul style="list-style-type: none"> • Appreciate the relevance of the course 	L1	
	Review of combinational and sequential design using SSI & MSI	<ul style="list-style-type: none"> • Review of EC202 	L2-L3	Design
	<i>Assignment I/Tutorial I</i>			
Digital implementation options	ASICs – Full custom, Semicustom (CBIC & MPGA), Programmable ASICs, standard parts, Comparison based on performance and cost, Design flow	<ul style="list-style-type: none"> • Evaluate approaches to digital system design and choose appropriate implementation option for the given specifications 	L4-L6	Comprehension
Digital system modeling	Domains – behavioral, structural, physical, levels of abstraction, Synthesis – high level, RTL level , logic synthesis, Hardware description languages	<ul style="list-style-type: none"> • Appreciate top-down design methodology, need for HDL, and choose level of abstraction for modeling the system 	L7-L8	Comprehension
VHDL	Entity and architectures, behavioral, data-flow and structural modeling, sequential and concurrent constructs, packages and libraries, VHDL styles for synthesis, Design case studies – combinational, sequential, FSM, RTL, arithmetic units, memory, simple uP	<ul style="list-style-type: none"> • Model a digital system using VHDL in behavioral, dataflow or structural domain 	L9-L26	Design
	<i>Assignment II/Tutorial II</i>			
	<i>Mid semester exam (L1-L26)</i>			

Programmable ASICs	Architecture of CPLDs and FPGAs, Antifuse, SRAM, EEPROM based technologies, Xilinx, Altera and Actel logic cells, I/O cells, Programmable Interconnect, Dynamic Reconfiguration	• Appreciate architecture of CPLDs and FPGAs, choose appropriate implementation option for the given specifications, implement the digital system using Xilinx FPGAs and verify the design	L27-L35	Analysis
	<i>Assignment III/Tutorial III</i>			
Embedded systems using FPGAs	Embedded system design concepts, Embedded cores on FPGAs, SoPC, Issues in embedded system design using FPGAs	• Appreciate issues in embedded system design using FPGAs	L36-L38	Analysis
Logic implementation for FPGAs	Logic synthesis, logic optimizations, Physical design for FPGAs, power optimization, system specification and codesign issues	• Logic design processes in FPGAs	L39-L41	Application, Analysis
Testing and verification	Functional and timing simulation, delay models, boundary scan, faults, fault simulation, BIST, DFT, Verification	• Appreciate the need for design for testability and evaluate options available for testing and verification of digital systems	L42-L44	Application, Analysis

10. Course web page : <http://172.16.200.9/~vc/>

11. Reference Books

<p>a) <i>M.J.S.Smith – ASICs, Pearson Education, 1997</i> b) <i>C.H. Roth, Digital system design using VHDL, PWS, 1998/2007</i> c) <i>Brown and Vranesic, Fundamentals of Digital logic with VHDL design, TMH, 2000</i> d) <i>W.Wolf, FPGA based system design, Pearson, 2004</i></p>	<p>e) <i>Clive Maxfield, The Design Warriors's Guide to FPGAs, Elsevier, 2004</i> f) <i>Peter Ashenden, The Designer's Guide to VHDL, Morgan Kaufman, 2002</i> g) <i>Peter Ashenden, VHDL 2007 & Digital Design using VHDL, Elsevier, 2007</i></p>
--	--

EVALUATION PLAN :

Mid semester exam - 25% Assignments/Quiz - 25%
End semester exam - 50%

Prepared by:

Approved by

Dr. Sumam David S.
Course Instructor

Dr. Sumam David S.
Head, Dept of E&C and DUGC Chairperson