COURSE PLAN AND EVALUATION PLAN

1. Course Code: EC200 2. Course Title: DIGITAL SYSTEM DESIGN
3. L – T – P**:** **3-1-0** 4. Credits**:** **4**
5. Pre-requisite**:** **-** 6. Teaching Department**:** **Electronics & Communication Engg.**
7. Course Instructor**:** **Dr SUMAM DAVID S.**
8. Course Outcomes:

At the end of the course the student must be able to

- Design combinational circuits using gates, multiplexer and decoders given a set of specifications
- Model combinational circuits using Verilog
- Design non-pipelined sequential circuits using specified/ available SSI & MSI devices given a set of specifications
- Model sequential circuits using Verilog

9. Course Coverage

Module	Contents	Objectives	Lecture	Evaluation
Introduction	Introduction to DSD – Objectives of the course, motivation, course plan, evaluation method, references	Appreciate the relevance of the course	**L1**	
Introduction to logic circuits	Logic gates, Boolean algebra, Sum of products and product of sums forms, Combinational circuit analysis, Minimisation techniques – K map, Combinational circuit synthesis using gates, Introduction to CAD tools, Introduction to Verilog, Other combinational minimization techniques	Design combinational circuits using gates given a set of specifications Describe combinational circuits using Verilog HDL	**L2 – L9**	**Design**
	Assignment I/Tutorial I			
Number systems & codes	Positional number systems, representation of negative numbers, binary arithmetic – addition, subtraction, multiplication, Design of arithmetic circuits using Verilog	Represent and perform arithmetic using binary number system Describe arithmetic circuits using Verilog HDL	**L10 – L15**	**Design**
	Assignment II/Tutorial II			

Combinational logic design	Combinational circuit design using MSI –Multiplexers, Decoders, comparator, priority encoder, Code converters, Design of combinational circuits using Verilog	Design combinational circuits using specified/ available SSI & MSI devices given a set of specifications Describe a combinational system using Verilog HDL	**L16-L21**	**Design**
	Assignment III/Tutorial III			
Digital logic families	Logic families, Characteristics of CMOS, Properties of logic elements: Delays - tplh, tphl, Rise time, fall time, Propagation delays; Noise Margin. Hazards – static and dynamic, tristate logic	Appreciate the features of digital logic families	**L22-L23**	**Comprehension**
Flip flops, registers and counters	Latches and flip flops, Setup and Hold time, Clock period and frequency, counters, shift registers, Using Verilog constructs for registers and counters	Design of counters given a set of specifications Describe a synchronous counter using Verilog HDL	**L24 – L29**	**Design**
	Assignment IV/Tutorial IV			
Sequential logic design	State Machine analysis, Finite state machine design, ASM charts, state minimization, state assignment, synthesis using D-FF and JK-FF, Design of sequential circuits using Verilog, linked state machines	Design sequential circuitsgiven a set of specifications Describe sequential circuits using Verilog HDL	**L30 – L37**	**Design**
	Assignment V/Tutorial V			
Register Transfer level design	Datapath and control path, Serial adder, shift and add multiplier, Division, RTL modeling using Verilog	Model non-pipelined sequential circuits using RTL approach in Verilog	**L37 – L42**	**Design**

10. Reference Books

Stephen Brown, Zvonko Vranesic, Fundamentals of Digital logic with Verilog design, MGH, 2014 *Morris Mano, MD Ciletti, Digital design with an introduction to Verilog, Pearson, 2015* *Ming-Bo Lin, Digital System, Designs and Practices using Verilog HDL and FPGAs, Wiley 2012*	*J.F.Wakerly, Digital Design Principles and Practices, PH, 1999.* *D.D. Givone, Digital Principles and Design, TMH, 2002* *J. Bhaskar, A Verilog HDL Primer, BSP, 2008* *NPTEL lectures on Digital Systems*

EVALUATION PLAN:

Mid semester exam - 25% Continuous assessment - 25% End semester exam - 50%

Prepared by: Approved by

Prof. Sumam David S. Prof Ramesh Kini

Course Instructor Head, Dept of E&C and DUGC Chairperson