COURSE PLAN AND EVALUATION PLAN

1. Course Code: EC204
2. Course Title: DIGITAL SYSTEM DESIGN LAB
3. L – T – P**:** **0-0-3**
4. Credits**:** **2**
5. Co-requisite**:** **EC200**
6. Teaching Department**: Electronics & Communication Engg.**
7. Course Instructor**:** **Dr SUMAM DAVID S.**
8. Course Objectives:
   Develop digital circuit design, analysis, implementation and debugging skills
   Develop good design practises used in digital systems
   Introduce HDL for design of digital systems
9. Course outcomes
   At the end of the program the student must be able to

   Design combinational circuits using SSI and MSI ICs and test it using simulation tools
   Design combinational circuits using Verilog and verify using simulation
   Design non-pipelined sequential circuits using SSI & MSI ICs and test it using simulation tools
   Design non-pipelined sequential circuits using Verilog and verify using simulation

10. Course Coverage (12 – Lab Schedule) **:**

Module	*Content*	*After completing this chapter, the student will be able to*	*No of weeks*	*Evaluation*
Familiarisation to design environment	Introduction to digital system modelling using		1	
Combinational circuit design	Design and implementation of adders, comparators, decoders, priority encoders, multiplexers, and multi-bit adders	Design, implement & test combinational circuits using Logisim Design, implement & simulate combinational circuits using Verilog	4	Test I

Sequential circuit design	Design and implementation of counters, shift registers, sequence detectors, simple state machines for applications like traffic light control, digital lock, vending machine etc.	Design, implement & test simple sequential circuits using Logisim Design, implement & simulate simple sequential circuits using Verilog	5	Test II
RTL design	Design of serial adder and shift and add multiplier using RTL approach	Model digital systems using RTL approach in Verilog	2	

11. EVALUATION PLAN:

Mid semester exam - 20% Continuous assessment - 50% End semester exam - 30%

Prepared by: Approved by

Prof. Sumam David S. Prof Ashvini Chaturvedi
Course Instructor Head, Dept of E&C and DPGC Chairperson