COURSE PLAN AND EVALUATION PLAN

1. Course Code: EC204 2. Course Title: DIGITAL SYSTEM DESIGN LAB

3. L-T-P: **0-0-3** 4. Credits: **2**

5. Co-requisite: EC200 6. Teaching Department: Electronics & Communication Engg.

7. Course Instructor: Dr SUMAM DAVID S. & Dr. LAISHRAM THOIBILEIMA CHANU

8. Course Objectives:

Develop digital circuit design, analysis, implementation and debugging skills

Develop good design practices used in digital systems

Model simple digital systems using HDL and implement using FPGAs

9. Course outcomes

At the end of the program, the student must be able to

Design and test combinational circuits using SSI and MSI ICs

Design and simulate combinational circuits using Verilog and implement them on FPGA

Design and test non-pipelined sequential circuits using SSI & MSI ICs

Design and simulate non-pipelined sequential circuits using Verilog and implement them on FPGA

10. Course Coverage (12 – Lab Schedule):

Module	Content	After completing this chapter, the student	No of weeks	Evaluation
		will be able to		
Combinational circuit	Design and implementation of adders,	Design, implement & test combinational	5	Test I
design	comparators, decoders, priority encoders,	circuits using SSI and MSI ICs		
	multiplexers, and multi-bit adders	Design and simulate combinational circuits		
		using Verilog and implement on FPGA		

Sequential circuit	Design and implementation of counters,	Design, implement & test simple sequential	5	Test II
design	shift registers, sequence detectors, simple	circuits using SSI & MSI ICs & Logisim		
	state machines for applications like traffic	Design and simulate simple sequential		
	light control, digital lock, vending machine	circuits using Verilog and implement on		
	etc.	FPGA		
RTL design	Design of serial adder and shift and add	Model digital systems using RTL approach	2	
	multiplier using RTL approach	in Verilog		

11. EVALUATION PLAN:

Mid semester exam - 30% Continuous assessment - 40% End semester exam - 30%

Prepared by: Approved by

Prof. Sumam David S.

Course Instructor

Prof Ramesh Kini M.

Head, Dept of E&C and DPGC Chairperson