COURSE PLAN AND EVALUATION PLAN

1. Course Code: EC340
2. Course Title: **COMPUTER ORGANIZATION AND ARCHITECTURE**
3. L – T – P**:** **3-1-0**
4. Credits**:** **4**
5. Pre-requisite**:** Digital System Design
6. Teaching Department**:** **Electronics & Communication Engg.**
7. Course Instructor**:** **Dr SUMAM DAVID S.**
8. Objectives of the Course:

At the end of the course the student must be able to

- Understand the architecture of a basic computer system and its components, and the role of performance in designing computer systems
- Understand how to design an instruction set and its impact on processor design.
- To design ALU. processor data path and control path
- Design pipeline processor including data path and control path, and design to detect and resolve hazards.
- Understand memory hierarchy design and its impact on overall processor performance. Design cache memory based on the characteristics of the expected workload. Understand secondary storage organization

Course Coverage**:**

Module	Contents	Objectives	Lecture	Evaluation
Introduction	Introduction to COA – Objectives of the course, motivation, course plan, evaluation method, references, Digital implementation options	• Appreciate the relevance of the course	**L1**	
	Review of combinational and sequential design	• Review of Digital System Design	**L2-L5**	**Design**
	Components of a computer system. Evolution of Technology. Factors affecting computer systems design (e.g., technology, applications, performance requirements)	• Understand architecture of a basic computer system and its components, role of performance in designing computer systems	**L6 – L7**	**Comprehension**
Instruction Set Architecture	The role of an instruction set. interface between hardware and software; issues to consider when designing an instruction set; addressing modes.	• Understand how to design an instruction set and its impact on processor design	**L8-L10**	**Comprehension**
Arithmetic and Logic Units (ALU) for computers	Number system, addition and subtract, adders; multiplication and multipliers; division and dividers; floating point numbers and floating point units	• To Implement arithmetic algorithms	**L11-L18**	**Design**

Processor Design	Data path and control; single cycle design and implementation; simplifying control design; multicycle implementation of data path and control	• To implement datapath and control path of processors	**L19-L24**	**Analysis**
Pipelining	Basic concepts in pipelining; data path for pipeline processor implementation, data hazard and forwarding, data hazard and stalling; control design for pipelines, Scheduling (static and dynamic) and forwarding to reduce/ minimise pipeline stalls	• Implement a minimal RISC ISA (MIPS) pipeline • Examine techniques to improve pipeline efficiency	**L25-L30**	**Design**
Instruction level parallelism	Instruction level parallelism and its dynamic exploitation – dynamic scheduling, hardware speculation, Exploiting instruction level using software approaches – static branch prediction, VLIW, hardware support, Limits of Instruction level parallelism	• Examine hardware and software techniques for ILP • Limits of ILP	**L31-L36**	**Analysis**
Memory Hierarchy	Cache memories. Introduction to caches, measuring and improving performance of caches; design alternatives, direct map, associative caches; replacement policies Virtual Memory: basic design, address translation, placement and replacement; cost and performance	• Examine techniques to improve memory management	**L37-L42**	**Design**

9. Course web page : Moodle on iris

10. Reference Books

a) David Patterson and John Hennessy, Computer Organization and Design, The hardware software interface, Elsevier, 5th edition, 2014
b) Carl Hamacher, Z. Vranesic, S. Zaky, N. Manjikian, Computer Organisation and Embedded Systems, Mc Graw Hill, 6th edition, 2012
c) John Hayes, Computer Architecture and Organization, McGraw Hill, 3rd edition, 2017
d) David Patterson and John Hennessy, Computer Architecture - A Quantitative Approach, Morgan Koufmann, 6th Edition, 2019
e) NPTEL courses on Computer Architecture

EVALUATION PLAN :

Mid semester exam - 20% Continuous assessment - 50% End semester exam - 30%

Prepared by:

Dr. Sumam David S.
Course Instructor

Approved by

Prof T. Laxminidhi
Head, Dept of E&C and DPGC Chairperson