COURSE PLAN AND EVALUATION PLAN

1. Course Code: EC340
2. Course Title: **COMPUTER ORGANIZATION AND ARCHITECTURE**
3. L – T – P**:** **3-1-0**
4. Credits**:** **4**
5. Pre-requisite**:** Digital System Design
6. Teaching Department**:** **Electronics & Communication Engg.**
7. Course Instructor**:** **Dr SUMAM DAVID S.**
8. Course Outcomes

On successful completion of the course, the student will be able to

CO1 Understand the architecture of a basic computer system and its components, and the role of performance in designing computer systems
CO2 Understand memory hierarchy design and its impact on overall processor performance
CO3 Design ALU, processor data path and control path
CO4 Design pipeline processor including hazard detection logic

Course Coverage**:**

Module	Contents	Objectives	Lecture	Evaluation
Introduction	Introduction to COA – Objectives of the course, motivation, course plan	• Appreciate the relevance of the course	**L1**	
	Review of combinational and sequential design	• Review of Digital System Design	**L2-L4**	**Design**
	Components of a computer system. Evolution of Technology. Factors affecting computer systems design (e.g., technology, applications, performance requirements)	• Understand architecture of a basic computer system and its components, role of performance in designing computer systems	**L5 – L6**	**Comprehension**
Instruction Set Architecture	The role of an instruction set. interface between hardware and software; issues to consider when designing an instruction set; addressing modes.	• Understand how to design an instruction set and its impact on processor design (RISC-V)	**L7-L9**	**Comprehension**
Arithmetic and Logic Units (ALU) for computers	Number system, addition and subtract, adders; multiplication and multipliers; division and dividers; floating point numbers and floating point units	• To implement arithmetic algorithms	**L10-L15**	**Design**
Processor Design	Data path and control; single cycle design and implementation; simplifying control design; multicycle implementation of data path and control	• To implement datapath and control path of processors (RISC-V)	**L16-L21**	**Analysis**

Pipelining	Basic concepts in pipelining; data path for pipeline processor implementation, data hazard and forwarding, data hazard and stalling; control design for pipelines, Scheduling (static and dynamic) and forwarding to reduce/ minimise pipeline stalls	• Implement a minimal RISC ISA (RISC-V) pipeline • Examine techniques to improve pipeline efficiency	**L22-L27**	**Design**
Memory Hierarchy	Cache memories. Introduction to caches, measuring and improving performance of caches; direct map, associative caches; replacement policies Virtual Memory: basic design, address translation, placement and replacement; cost and performance	• Examine techniques to improve memory management	**L28-L33**	**Design**
Instruction-level parallelism (ILP)	ILP and its dynamic exploitation – dynamic scheduling, hardware speculation, Exploiting ILP using software approaches – static branch prediction, VLIW, hardware support, Limits of ILP	• Examine hardware and software techniques for ILP • Limits of ILP	**L34-L39**	**Analysis**
Data Level and Thread Level Parallelism	Data Level Parallelism – Vector, SIMD, VLIW, GPU architectures, Thread level parallelism, centralized shared memory architectures, memory consistency issues	• Examine ways to improve processor performance by exploiting Data and thread-level parallelism.	**L40-L42**	**Analysis**
Current trends in microprocessor architectures	Issues in applications (optimizing the hardware – software interface), Domain-specific architectures, reconfigurable computing	Appreciate current trends in VLSI architecture	**L43-L44**	**Comprehension**

9. Course web page : Moodle on iris

10. Reference Books

a) David Patterson and John Hennessy, Computer Organization and Design RISC V Edition: The Hardware/Software Interface, MK, 2nd edition, 2021
b) Carl Hamacher, Z. Vranesic, S. Zaky, N. Manjikian, Computer Organisation and Embedded Systems, Mc Graw Hill, 6th edition, 2012
c) John Hayes, Computer Architecture and Organization, McGraw Hill, 3rd edition, 2017
d) David Patterson and John Hennessy, Computer Architecture - A Quantitative Approach, MK, 6th Edition, 2019
e) NPTEL courses on Computer Architecture

EVALUATION PLAN : Mid semester exam - 20% Continuous assessment - 40% End semester exam - 40%

Prepared by:

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Approved by

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