COURSE PLAN AND EVALUATION PLAN

1. Course Code: EC806
2. Course Title: DIGITAL DESIGN USING FPGAS
3. L – T – P**:** **2-0-3**
4. Credits**:** **4**
5. Pre-requisite**:** Digital Electronics
6. Teaching Department**:** **Electronics & Communication Engg.**
7. Course Instructor**:** **Dr SUMAM DAVID S.**
8. Objectives of the Course:

At the end of the program the student must be able to

Design digital systems and model using HDL, given a set of specifications
Implement digital systems using FPGAs – As the course is offered online this semester it may not be possible to carry out the lab exercises (highlighted in course plan) involving implementation and testing on FPGA board. Students will have the opportunity to try them on the FPGA boards when they report to Department

9. Course Coverage**:**

Module	Contents	Objectives	Lecture/ Lab	Evaluation
Introduction	Introduction to DSD – Objectives of the course, motivation, course plan, evaluation method, references, Digital implementation options	• Appreciate the relevance of the course	**L1**	
	Review of combinational and sequential design using SSI & MSI	• Review of Digital Electronics	**L2-L5**	**Design**
Digital system modeling	Domains – behavioral, structural, physical, levels of abstraction, Synthesis – high level, RTL level , logic synthesis, Hardware description languages	• Appreciate top-down design methodology, need for HDL, and choose level of abstraction for modeling the system	**L6 – L7**	**Comprehension**
Familiarisation to design environment	Introduction to digital system modelling using FPGA Design Environment	• Using design tools to describe a digital system using Verilog HDL, simulate its functionality, implement & test the design by downloading to FPGA	**P1**	
Verilog	Modelling Combinational, Sequential, FSM, Design case studies, styles for synthesis, test benches,	• Model a digital system using Verilog HDL	**L8-L15**	**Design**
Programmable ASICs	Architecture of CPLDs and FPGAs, Antifuse, SRAM, EEPROM based technologies, Xilinx, Altera and Actel logic cells, I/O cells, Programmable Interconnect, Dynamic Reconfiguration	• Appreciate architecture of CPLDs and FPGAs, choose appropriate implementation option for the given specifications	**L16-L20**	**Analysis**

Combinational circuit design	Design of decoders, priority encoders, multiplexers, multi-bit adders and comparators	• Design, implement & test combinational circuits using FPGAs	**P3-4**	**Design**
Sequential circuit design	Design of counters, shift registers, sequence detectors, implementation of state machines for applications like traffic light control, digital lock, vending machine etc.	• Design, implement & test simple sequential circuits using FPGAs	**P5-7**	**Design**
Mid semester exam				
Verilog	Design case studies – arithmetic units, memory, simple uP	• Model a digital system using Verilog HDL	**L21-27**	
RTL Design	Design of arithmetic units, simple uP	• Design, implement and test on FPGAs	**P8-9**	
Interfacing IO devices	Interfacing IO modules and peripheral devices to FPGA board	• Design, & interface peripheral devices to the FPGA board	**P8-P9**	**Design**
Embedded systems using FPGAs	Embedded system design concepts, Embedded cores on FPGAs, SoPC, Issues in embedded system design using FPGAs	• Appreciate issues in embedded system design using FPGAs	**L28-L32**	**Analysis**
	Implementation of embedded systems on FPGA	• Implement a simple embedded system on FPGA	**P10**	
Design Project	Implementing a digital system using FPGA board	Use FPGA for a signal processing or embedded application	**P10-P14**	**Design**

10. Course web page : Moodle on iris

11. Reference Books

a) M.J.S.Smith – ASICs, Pearson Education, 1997
b) C.H. Roth & L.K. John, Principles of Digital system design using Verilog, Cengage, 2016
c) M D Ciletti, Modelling, Synthesis and Rapid Prototyping with Verilog HDL, Pearson, 1999
d) M D Ciletti, Advanced Digital Design with Verilog HDL, Pearson, 2010
e) W.Wolf, FPGA based system design, Pearson, 2005
f) Peter Ashenden, Digital Design, An embedded systems approach using Verilog, Elsevier, 2008
g) https://people.ece.cornell.edu/land/courses/ece5760/FinalProjects/

EVALUATION PLAN :

Mid semester exam	- 20%	Quiz & Lab assessment	- 50%
Design Project	- 0 %	End semester exam	- 30%

Prepared by:

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Approved by

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