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Accurate estimation of decay coefficients for dynamic range compressors in hearing aids and a hardware level comparison of different architectures

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ABSTRACT

Dynamic Range Compression (DRC) algorithm helps to protect the residual hearing ability of hearing aid users by compressing the signal levels which go above a particular threshold. This paper addresses two different aspects of DRC for hearing aid applications. In the first part, methods to estimate the decay coefficients corresponding to the required time constants for a feed-forward DRC architecture accurately, to meet the hearing aid specifications are proposed. The effect of compression on the attack and release time parameters are compensated with the new formula. The hardware implementation of four different DRC architectures is explained in the second part of the paper. The estimated decay coefficients for a test signal were used for the corresponding hardware implementations and verified the validity of proposed algorithmic modifications. The architectures were implemented using UMC 65 nm standard cell libraries and the power and error results were compared. The proposed methods to estimate the decay coefficients for both attack and release phases show close to 0 dB error from expected output values, while conventional methods are not meeting the specifications. Hardware implementation shows that there is not much improvement in power performance, between a lower resolution Look-Up Table (LUT) based logarithm implementation and a higher resolution one. From the results, we propose using the absolute level detector based DRC with higher resolution logarithm without a gain smoothing stage at the output for lowest power consumption and better approximation error performance.

1. Introduction

Dynamic Range Compression (DRC) algorithm is used to bring down the dynamic range of normal audible sounds to the reduced range of hearing impaired persons. People with sensory neural hearing impairment cannot hear low intensity sounds, whereas their upper threshold of hearing will stay unaltered. Dynamic Range Compressor protects the residual hearing of such individuals by compressing the output signal level crossing a threshold after applying the prescribed gain. The rate at which the compression is to be applied and removed is decided by the time constants termed as attack and release time. Based on these time constants, the values of the envelope tracking decay coefficients are calculated. In general purpose DRC algorithms, the coefficients are estimated based on input signal level, whereas, in hearing aid specifications, the attack and release time constants are defined in terms of output signal level [1]. If the input signal level based coefficient estimation method is followed, the compression applied at the gain stage alters the expected value of the time constants considerably. Hence modifications are to be made in the estimation of decay coefficients to get an accurate measure of the output signal at the expected instant of time. Not much information is available in the literature regarding the hardware implementation of DRC algorithms. Different DRC architectures for which the time constant dependent parameter estimation methods are modified, are implemented using semi custom design flow and power and error performance are evaluated to choose the best one for low power hearing aid applications.

The effect of time constants on speech intelligibility has been an interesting topic among researchers for a long time. One such study is reported in a paper published by Blesser[2] in 1969. A long release time and short attack time are preferred for better speech quality where, the gain can decrease rapidly, and recover slowly. At the same time, attack time should be long enough to avoid transients. Even small differences in attack time can cause damage to the spectral contrast and speech intelligibility in the case of hearing aids [3]. Neuman *et al.* studied the effect of release

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time on sound quality using different compression ratios with different background noise [4], [5]. It has been observed that different release times give different levels of pleasantness with different combinations of compression factors and background noise. A detailed comparison of slow-acting and fast-acting compressors based on subjective tests are given in Stone et al. [6]. Fast attack time is needed in the range of 1 ms to 10 ms to protect the users from intense transient sounds like a door slamming or cup falling. The discussions on the merits and demerits of fast-acting compressors or syllabic compressors, i.e., attack time in the range of 2–10 ms and release time in the range of 20–150 ms diverge. Speech in quiet situations can be understood better for a wider dynamic range using syllabic compressors. Subjective studies show that syllabic compressors, affect the intelligibility adversely in noisy environments [7]. At the same time, some studies conclude that fast-acting multichannel compression improves the speech intelligibility in noisy backgrounds having spectral and temporal dips [8]. So a better control over the time constants is important to make the hearing aid output more intelligible in different situations.

McNally [9] explains the basic concepts of digital DRC algorithm. The author has studied the artifacts that can be created by the quantization errors at various stages of hardware implementation and recommends a smoothing stage to reduce it. The algorithm was tested on the COPAS2 processor, but the impact of power overhead and the change in effective time constants due to second stage filtering were not considered. Floru [10] compared the feed-forward and feed-back topologies in the analog domain and the gain equations were derived. The digital domain comparisons of the respective topologies are done in Abel et al. [11] and feed-forward topology is preferred over feed-back as it provides better stability and higher dynamic range [12]. Therefore feed-forward topology is used in this paper for our study. There are very few recent papers on dynamic range compressors for hearing aid applications. Chang et al. [13] describes the hardware implementation of DRC algorithm with the smoothing stage. The input level was estimated using a common time constant for both attack and release phases and the effect of double stage filtering on time constants and the final output is not discussed. Details of implemented architectures and result analysis were not given in the paper. Giannoulis [12] has done a study of various techniques in DRC and observed the lag in the release phase but did not propose any modification to overcome it. The effect of compression factor on the estimated attack time decay coefficients is studied in [14] and modifications are proposed in the calculation of it based on a look-up table generated from simulations to get expected output at the required time constants.

The detailed development of the algorithm and the proposed methods to estimate the accurate attack and release phase decay coefficients to meet the required time constant specifications given in the ANSI S3.22 standards for hearing aids are presented in this paper. Hardware implementation of the proposed modifications to the algorithm was carried out using different architectural approaches and the power and error performance at ASIC level implementation using UMC 65 nm standard cell libraries were compared.

In practical DRC algorithms, the gain is applied in the log domain and there are various methods for implementing logarithms on hardware. We used a direct look-up table method [13], since it is fast and consumes low power [15]. A comparison of quantization errors introduced by log tables of different resolutions is given in [13]. However, the authors have not given any analysis of the impact of the smoothing stage along with the log tables. Once the log resolution decreases, the quantization error increases, and the need for the smoothing stage increases.

The paper is organized as follows: basic concepts of DRC is explained in Section 2. In Section 3, the modifications to the algorithm with respect to hearing aid specifications are discussed. Details of hardware implementation are given in Section 4. Simulation results and conclusion are given in Sections 5 and 6, respectively.

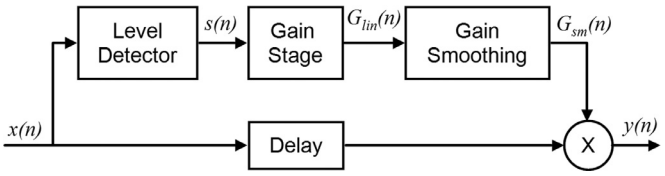


Fig. 1. Basic block diagram of a feed-forward DRC.

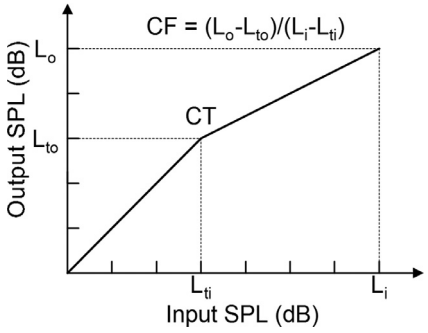


Fig. 2. Static compression curve in log domain.

2. Basics of DRC algorithm

Dynamic Range Compressors have two stages of processing- A level detection stage and a gain stage. There can be a smoothing stage also to reduce the unwanted wordlength error of hardware approximations [9]. Block diagram of a feed-forward DRC topology is shown in Fig. 1. The level detector estimates the incoming signal level. Depending on the input signal level, gain stage calculates the amount of compression to be applied based on an input-output(I/O) curve, which will be obtained from different gain prescription formulas corresponding to the particular audiogram of the hearing impaired person. A sample I/O curve is shown in Fig. 2 in which the input and output Sound Pressure Level (SPL) are specified in decibel (dB). I/O curve is defined by the static characteristics: Compression Threshold (CT) and Compression Ratio (CR). CT decides the level at which the compression is to be applied and CR is the ratio of change in input SPL to change in output SPL [1]. Compression Factor (CF) is the reciprocal of compression ratio, i.e., change in output SPL to change in input SPL. According to ANSI S3.22 specifications for hearing aids, the attack time is defined as the time it takes to reach within 3 dB of the final value of the output for an input signal changing from 55 dB to 90 dB. Release time is the time it takes to reach within 4 dB of the final value for an input changing from 90 dB to 55 dB [1].

3. Proposed modifications to the algorithm for estimation of decay coefficients

3.1. Level detection

The incoming signal level can be detected based on its absolute amplitude or the Root Mean Square (RMS) value. A low pass single pole Infinite Impulse Response (IIR) filter is used to estimate the signal averaged over a period depending on attack or release time constants. The input to the filter can be either the instantaneous absolute value (absolute detector) or the squared value of the input

signal level (RMS detector). In the case of an absolute detector [16]:

$$p(n) = \begin{cases} \alpha p(n-1) + (1-\alpha)|x(n)|, & \text{if } |x(n)| \geq p(n-1) \\ \beta p(n-1) + (1-\beta)|x(n)|, & \text{if } |x(n)| < p(n-1) \end{cases} \quad (1)$$

For RMS detector:

$$p(n) = \begin{cases} \alpha p(n-1) + (1-\alpha)x^2(n), & \text{if } x^2(n) \geq p(n-1) \\ \beta p(n-1) + (1-\beta)x^2(n), & \text{if } x^2(n) < p(n-1) \end{cases} \quad (2)$$

where α and β are attack and release phase decay coefficients. $x(n)$ is the input signal amplitude at n^{th} sample instant and $p(n)$ is the corresponding input SPL in linear scale. α is obtained in conventional methods by equating the unit step response of the above filters to −3 dB [16] as specified in Section 2.

$$1 - \alpha^{N_a+1} = 10^{-3/20} \quad (3)$$

If a similar method is followed, and by using the theory of transients [17], then β can be obtained by equating the unit step response to −4 dB of the final value as:

$$\beta^{N_r+1} = (10^{((CT+4)/20)} - 10^{FV/20})/(10^{IV/20} - 10^{FV/20}) \quad (4)$$

It is to be noted that the system will be in the release phase, only until the estimated input SPL crosses the compression threshold, *CT*. *IV* and *FV* are initial and final values of input SPL in dB. Number of samples, N_a and N_r corresponding to required attack and release time constants, t_a and t_r respectively, are obtained as,

$$N_a = f_s * t_a \quad (5)$$

$$N_r = f_s * t_r \quad (6)$$

where, f_s is the sampling frequency.

In the gain stage, the compression is applied in the log domain. So the input level measured in the linear domain is converted to log domain as

$$s(n) = 20\log_{10}(p(n)) \quad (7)$$

in the case of absolute detector and

$$s(n) = 10\log_{10}(p(n)) \quad (8)$$

in the case of RMS detector.

3.2. Gain calculation

Gain stage calculates the compression to be applied based on the input level detected in the previous stage. The gain equation is obtained from I/O curve for a feed-forward compressor as follows [11] :

$$G_{dB}(n) = (CF-1)(s(n) - CT) \quad (9)$$

$$G_{lin}(n) = 10^{(G_{dB}(n)/20)} \quad (10)$$

where G_{dB} and G_{lin} are the calculated gain in log and linear domains respectively. The delayed input signal is multiplied with the estimated gain to get the final output, $y(n)$.

$$y(n) = G_{lin}(n)x(n-D) \quad (11)$$

where D is the total processing delay of the entire DRC system.

3.3. Effect of compression factor on decay coefficients, α and β and proposed modifications to compensate the effect

It can be observed from Eq. (10) that the gain is related to input SPL, $s(n)$, by a factor $(CF-1)$. This effect of *CF*, on $s(n)$ causes the output to reach the expected value faster than the desired time constants, t_a and t_r. In our previous paper [14], a LUT based empirical method was proposed to compensate for this effect in the attack phase.

Accurate estimation of the decay coefficients α and β can be obtained by the following equations:

$$1 - \alpha^{N_a+1} = 10^{(-(3+\delta_a)/20)} \quad (12)$$

$$\beta^{N_r+1} = (10^{((CT+4+\delta_r)/20)} - 10^{FV/20})/(10^{IV/20} - 10^{FV/20}) \quad (13)$$

where, the values of offsets δ_a and δ_r are obtained as:

$$\delta_a = (FV-3) - \frac{(FV*(1-CF)-3)}{(1-CF)} \quad (14)$$

$$\delta_r = \frac{(CT*(1-CF)+4)}{(1-CF)} - (CT+4) \quad (15)$$

In the RMS detector, the output will reach steady-state faster since the input is squared. Accordingly, input SPL with offset should be squared in Eqs. (12) and (13)) for finding the decay coefficients for an RMS detector. The following equations will give accurate coefficients for an RMS detector.

For attack phase:

$$1 - \alpha^{N_a+1} = 10^{(-(3+\delta_a)/10)} \quad (16)$$

and for the release phase:

$$\beta^{N_r+1} = (10^{((CT+4+\delta_r)/20)} - 10^{FV/20})^2/(10^{IV/20} - 10^{FV/20})^2 \quad (17)$$

Consider the example in Fig. 3 of a particular test signal with *CT* and *CF* set as 70 dB and 0.5 respectively. Once the instantaneous input signal crosses *CT*, the system goes to attack phase. Output reaches within -3 dB of its final value when the input reaches within $-(3+\delta_a)$ of its final value, i.e., in this example, 84 dB with $\delta_a = 3$ for a compression factor of 0.5. The moment the instantaneous input intensity goes below the threshold value, the system goes to release phase but still under compression until $s(n)$ reaches *CT*. Output reaches −4 dB of its steady state value, i.e., in this case, 51 dB when $s(n) = (CT+4+\delta_r)$ which is 78 dB with δ_r=4 for a compression factor of 0.5.

In the case of above example, attack and release phase decay coefficients for an RMS detector can be obtained as given below.

$$1 - \alpha^{N_a+1} = 0.2512 \quad (18)$$

$$\beta^{N_r+1} = 0.0564 \quad (19)$$

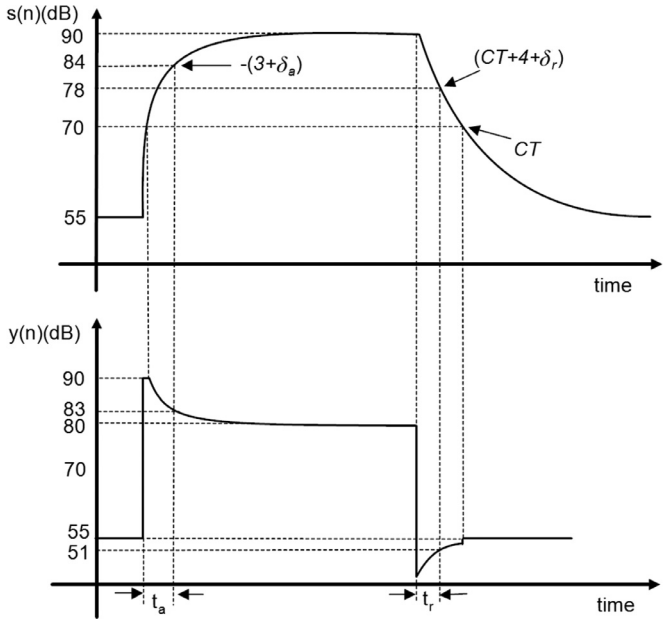


Fig. 3. Attack and release time plot corresponding to a sample estimated input curve s(n).

3.4. Smoothing

A smoothing filter can be used after converting the gain from the log domain to the linear domain to remove the approximation errors introduced at various stages of hardware implementation. The difference between smoothed gain and the actual gain is compared with an error threshold (G_{th}) and passed through a similar first order filter as in level detection.

$$G_{sm}(n) = \begin{cases} \alpha_{sm} G_{sm}(n-1) + (1-\alpha_{sm}) G_{lin}(n), \\ \quad \text{if } G_{sm}(n-1) - G_{lin}(n) \geq G_{th} \\ \beta_{sm} G_{sm}(n-1) + (1-\beta_{sm}) G_{lin}(n), \\ \quad \text{if } G_{sm}(n-1) - G_{lin}(n) < G_{th} \end{cases} \tag{20}$$

where α_{sm} and β_{sm} are the attack and release phase decay coefficients for smoothing stage. G_{sm} is the gain at the output of smoothing filter.

Since there is a new set of coefficients introduced in the smoothing stage, the output reaches its steady state slower than the actual expected value due to the impact of second stage filtering. If Eqs. (12) and (13) are used for coefficient estimation, then G_{lin} reaches within 3 dB and 4 dB points of its final values during the attack and release phases after $N_a + 1$ and $N_r + 1$ samples respectively. For example consider a test signal as in Fig. 3 which is sampled at 20 kHz and goes from 55 dB to 90 dB after 600 samples and from 90 dB to 55 dB after 1800 samples. Both attack and release time constants, t_a and t_r are chosen as 4 ms. Then N_a and N_r can be obtained as 80 samples from Eqs. (5) and (6). The magnitude curve obtained from MATLAB® simulations for G_{lin} in dB is plotted in Fig. 4. It can be observed that the gain curve reaches its 3 dB and 4 dB points (i.e., −7 dB and −4 dB corresponding to attack and release phases respectively, in the plot) after 81 samples each (i.e., at sample numbers 681 and 1881). In DRC with smoothing stage, second stage filtering is applied to this already filtered signal (G_{lin}), with a new set of co-efficients (α_{sm} and β_{sm}). It will further delay the final gain curve G_{sm}. The number of samples (N_{asm} and N_{rsm}) and the smoothing stage decay coefficients (α_{sm} and β_{sm}) are also related by transient equations similar to (3) and (4) as given below:

$$(10^{(IV_{Glin}/20)} - 10^{(FV_{Glin}/20)})\alpha_{sm}^{N_{asm}+1} + 10^{(FV_{Glin}/20)} = 10^{(FV_{Glin}+3)/20} \tag{21}$$

$$(10^{(IV_{Glin}/20)} - 10^{(FV_{Glin}/20)})\beta_{sm}^{N_{rsm}+1} + 10^{(FV_{Glin}/20)} = 10^{(FV_{Glin}-4)/20} \tag{22}$$

Here, there is no effect of CF, so δ offset is not required. The total time to reach the expected output values will be $(N_a + N_{asm})$ and $(N_r + N_{rsm})$ samples in the case of DRC with the smoothing stage incorporated.

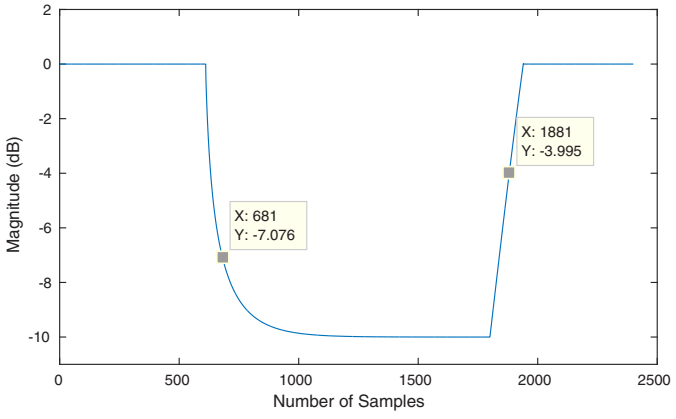


Fig. 4. Plot of Gain Curve for the test signal.

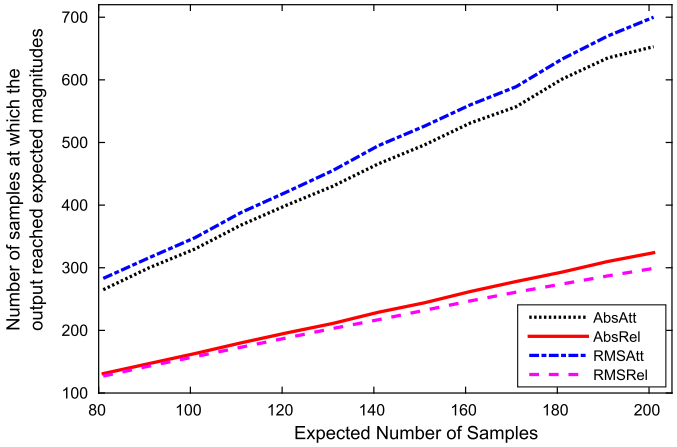


Fig. 5. Number of Samples plot for attack and release phases for finding the decay coefficients for smoothing stage. The legends can be interpreted as: *Abs*- Absolute detector based DRC; *RMS*- RMS detector based DRC; *Att*- Attack phase; *Rel*- Release phase.

The accurate expected output for DRC with the smoothing stage can also be obtained using an empirical method as follows. If same coefficients are used for both the level detection and smoothing stages instead of using two separate decay coefficients for two phases of filtering, it is observed that the combination follows a linear relation with the required single-stage time constant in both the attack and release phases in the case of the absolute detector. So new coefficients for DRC with smoothing stage incorporated can be obtained from the modified number of samples (N_{asm} for attack and N_{rsm} for release) as given below.

$$N_{asm} + 1 = 0.3039(N_a + 1) \tag{23}$$

$$N_{rsm} + 1 = 0.6177(N_r + 1) \tag{24}$$

In the case of RMS detector, there is no squaring effect in the smoothing stage compared to level detection. So if we use Eqs. (16) and (17) for the level detection stage and Eqs. (12) and (13) for the smoothing stage, a linear relationship can be obtained with respect to single-stage expected decay coefficients. So for the RMS detector with smoothing stage, accurate coefficients can be obtained from a modified number of samples as given below.

$$N_{asm} + 1 = 0.2872(N_a + 1) \tag{25}$$

$$N_{rsm} + 1 = 0.6500(N_r + 1) \tag{26}$$

The linear plots to get the constants in Eqs. (23)–(26) are obtained by varying the attack and release times from 4 ms to 10 ms, (expected number of samples from 81 to 201) as shown in Fig. 5 for a *CF* of 0.5 and a sampling frequency of 20 kHz. The X-axis is the expected number of samples and Y-axis shows the number of the sample at which the output reached the expected values using the decay coefficients derived from Eqs. (12) and (13). The ratios of these expected and the actual number of samples are used as constants in Eqs. (23)–(26) to get the modified number of samples N_{asm} and N_{rsm}.

4. Hardware implementation

The hardware architecture of the DRC algorithm with an absolute level detector is shown in Fig. 6. The total processing latency, *D* added to the input is constituted by registers at different stages. All the coefficients and threshold values are stored using programmable registers. The architecture is designed in such a way

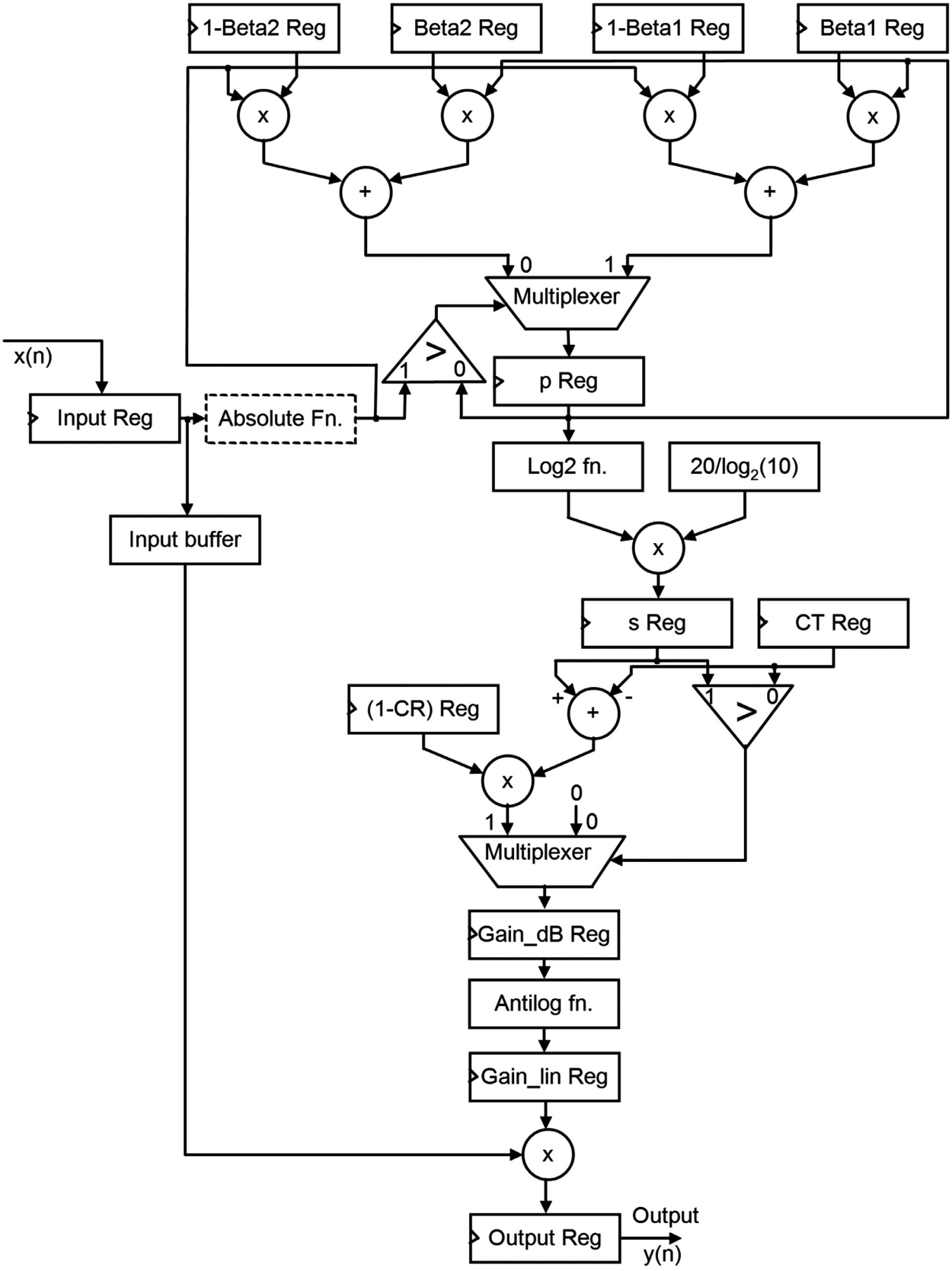


Fig. 6. Hardware architecture of the absolute detector based DRC algorithm.

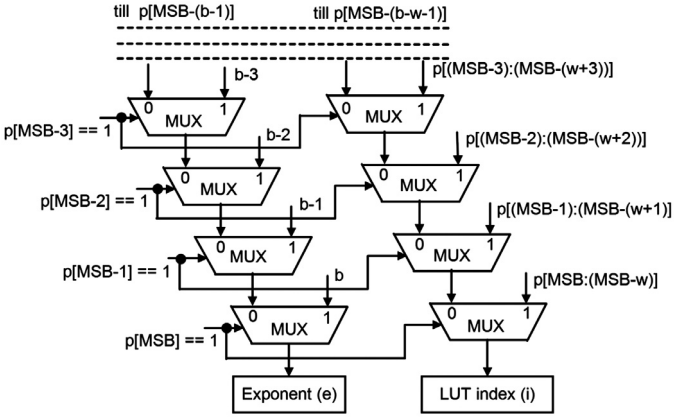


Fig. 7. Priority encoder based address generator used for logarithm table.

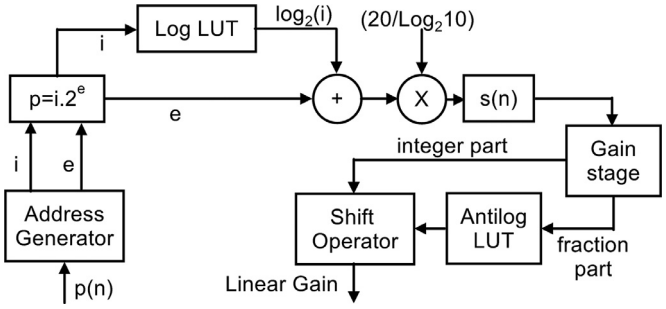


Fig. 8. LUT based logarithm implementation.

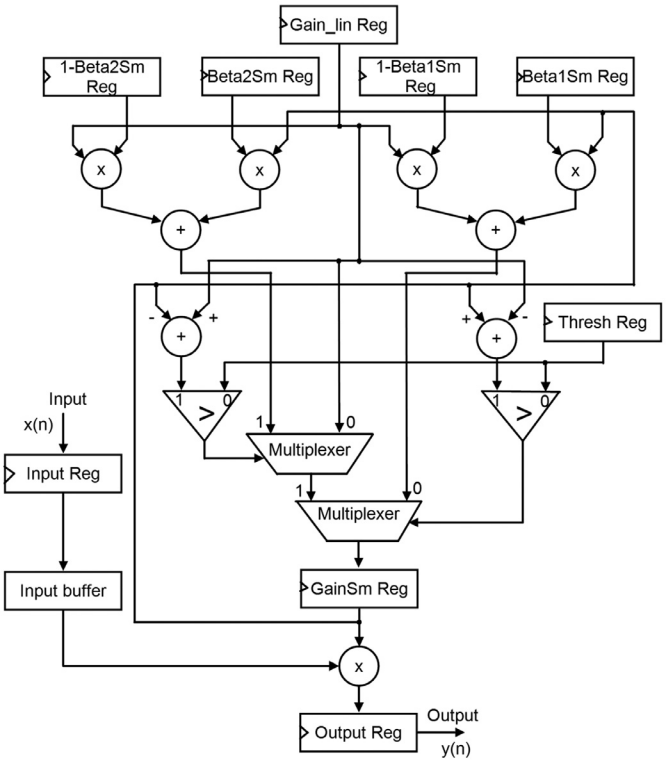


Fig. 9. Hardware architecture of the smoothing stage.

that the data will be loaded and processing starts once all the programmable parameters are stored in corresponding registers. Input and all the coefficient registers are represented using 16 bit fixed point arithmetic. In the case of absolute level detection based algorithm without the smoothing stage, five multiplications are needed including one constant multiplier. For RMS detector one extra multiplier is needed to get the squared value of the input signal.

The architectures are implemented with logarithm tables of 4 bit and 8 bit index resolution. Since the input is in 16 bit signed format, leading one's counter is used to reduce the input bit width to the log table index width. Block diagram of the logarithm implementation is shown in Fig. 8. Log table index (mantissa part of the measured input SPL) and the exponent parts are obtained from a priority encoder based address generator as shown in Fig. 7, where w represents the width of the log table index and b represents the number of stages present in the priority encoder. In the case of 4 bit resolution table, an extra four stages are needed for leading one detector compared to 8 bit resolution table. This increase in address detection hardware in turn nullifies the advantage of using a smaller Look Up Table (LUT) with lower depth and makes the power consumption for both the cases almost similar. But, as the LUT depth reduces, the quantization error increases. Hence, 8 bit resolution log table implementation gives better performance over 4 bit resolution log table considering both power and error values. In the case of RMS detector, *Absolute Fn.*, shown in the dotted box in Fig. 6 is replaced by the squaring stage. The input range to the LUT gets scaled up from 15 bit to 30 bits due to squaring. This results in 15 extra stages in leading one's counter and an effective increase in hardware complexity. We used base-2 logarithm and antilogarithm tables as it gives more efficient hardware implementation [15]. Base-2 log values are then converted to Base-10 by the scaling factor and used in the gain stage. The antilog value of the fractional part of gain in decibel was shifted according to the integer part to obtain the gain in the linear domain.

Hardware architecture of the smoothing stage is shown in Fig. 9. In the smoothing stage, the difference between the DRC estimated gain from the gain stage (G_{lin}) and the smoothed gain (G_{sm}) is compared with a gain error threshold value, G_{th}. If the difference is greater than G_{th}, the smoothing filter is applied. *Thresh_Reg*, the register used to store G_{th} shown in Fig. 9 is also 16 bit wide. Since one register is used to store the smoothed gain, the input buffer stage length increases by one. In smoothing stage, the major contribution of hardware complexity comes from two multipliers and two 16 bit subtractor based comparators along with the registers needed for storing smoothing filter coefficients, G_{th} and the final gain value.

5. Results and discussion

A step signal sampled at 20 kHz was selected as a test signal according to ANSI S3.22 specifications for hearing aids. The signal changes from 55 dB to 90 dB at 600th sample and comes back to 55 dB after 1800 samples, having enough time to reach steady state during both attack and release phases. Different attack and release phase decay coefficients are estimated using both conventional (Eqs. (3) and (4)) and proposed (Eqs. (12), (13), (16), (17) and (23)–(26)) methods for an attack and release time constant of 4 ms. The estimated coefficient values are given in Table 1.

Table 1
Attack and Release phase decay coefficients estimated using the modified algorithm for 4 ms transient period with a 20 kHz sampling frequency.

Parameter	Without smoothing		With smoothing	
	Abs	RMS	AbsSm	RMSSm
Attack time constant	0.9914	0.9964	0.9729	0.9714& 0.9880
Release time constant	0.9824	0.9651	0.9733	0.9746& 0.9498

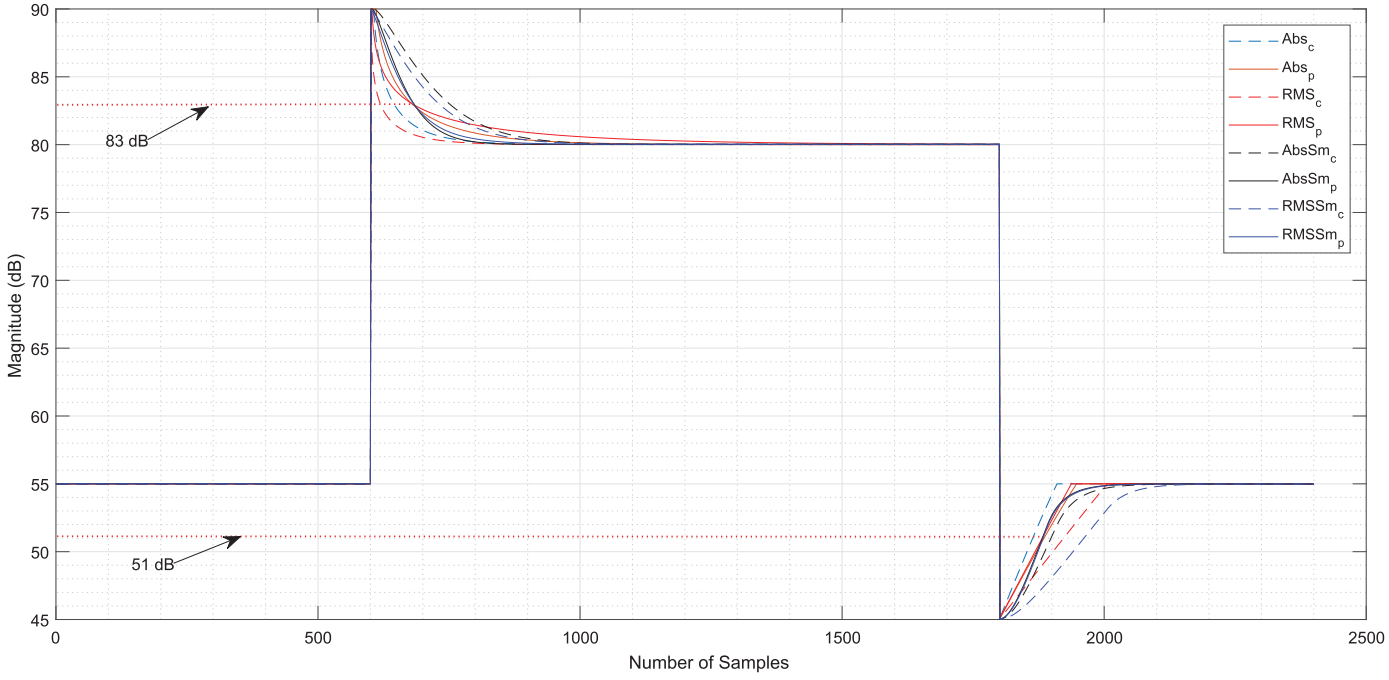


Fig. 10. Output waveforms for proposed (solid lines) and conventional (dashed lines) methods of decay coefficients estimation. (Figure legends can be interpreted as follows: *Abs* - Absolute detector based DRC; *RMS* - RMS detector based DRC; *Sm* - DRC with smoothing stage included; $_c$ - conventional method; $_p$ - proposed method).

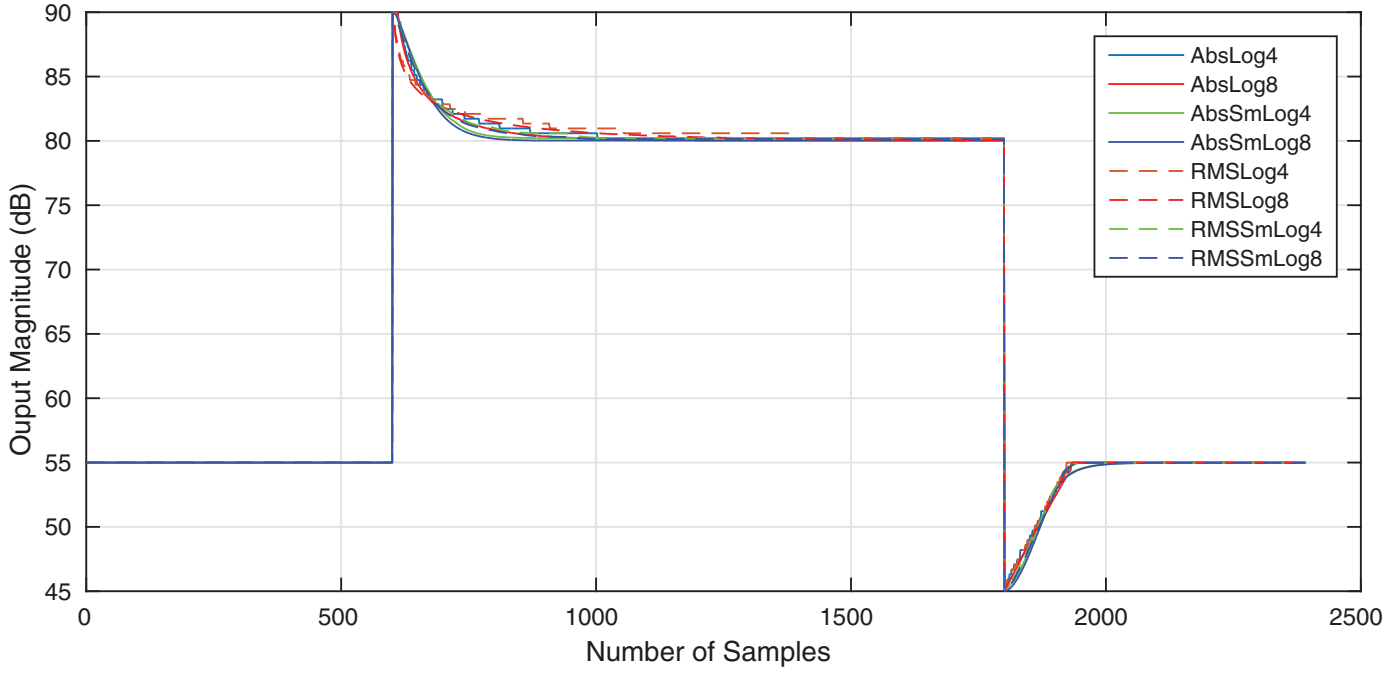


Fig. 11. Output waveforms after post layout simulation for different architectures.

All the simulations were carried out and proposed and conventional methods for coefficients estimation were verified using MATLAB® 2015.2.

The error table with proposed and conventional methods are given in Table 4. It can be observed that the proposed method gives error-free results while the conventional methods give errors as high as 3.06 dB. The output plots are shown in Fig. 10. The figure shows that proposed methods perform as expected while conventional methods are not giving expected results during both attack and release phases for all the test cases.

Table 2
Power consumption for different architectures.

Log table resolution	Without smoothing		With smoothing	
	Abs (µW)	RMS (µW)	AbsSm (µW)	RMSSm (µW)
4 bit	2.416	4.054	3.881	5.02
8 bit	2.568	4.292	4.055	5.194

Table 3
Synthesised gate count and area report.

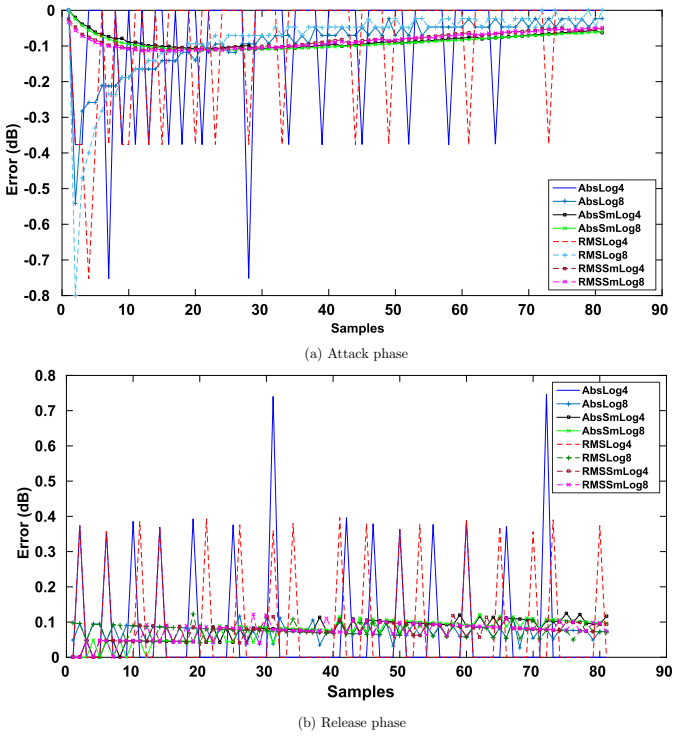
	Without smoothing				With smoothing			
	Abs		RMS		AbsSm		RMSSm	
	Log4	Log8	Log4	Log8	Log4	Log8	Log4	Log8
Gate count	6054	7195	9475	10,658	9035	10,303	12,537	13,025
Area (μm^2)	19,877	22,269	31,285	33,650	29,647	32,088	41,529	42,347

Table 4
Output errors using conventional and proposed methods for decay coefficients estimated from output signal for the transient period of 81 samples for attack and release phases.

Parameters	Without smoothing				With smoothing			
	Abs		RMS		AbsSm		RMSSm	
	conv	prop	conv	prop	conv	prop	conv	prop
Att. time const.	0.985	0.9914	0.985	0.9964	0.985	0.9729	0.985	0.9714&0.9880
o/p at 81st sample (dB)	81.47	83	86.06	83	80.75	83	85.16	83
Error (dB)	−1.53	0	3.06	0	−2.25	0	2.16	0
Rel. time const.	0.9763	0.9824	0.9763	0.9651	0.9763	0.9733	0.9763	0.9746&0.9498
o/p at 81st sample (dB)	52.548	51	49.533	51	48.96	51	47.27	51
Error (dB)	−1.548	0	1.467	0	2.04	0	3.73	0

5.1. Hardware implementation results

All four architectures were described using Verilog Hardware Description Language (HDL), synthesized, placed and routed with Cadence®Design tools using UMC 65 nm low power standard cell libraries. Clock frequency was chosen as 20 kHz which matches with the practical sampling frequency of hearing aids. Output waveforms for a CF of 0.5 and CT of 70 dB from post layout simulations are shown in Fig. 11. All the outputs reach the expected value of 83 dB during the attack phase and 51 dB during the release phase in 4 ms. Post-layout core power analysis was done using Cadence Voltus™ IC Power Integrity Solution with a constant switching activity and typical parasitic corner to get a uniform comparison of the architectures. All 4 architectures (i.e., DRC with absolute level detector and RMS level detector, without smoothing stage included and with smoothing stage) were compared with 4 bit and 8 bit resolution LUT based logarithm and antilogarithm implementation. Post layout power results are given in Table 2. From Table 2, it can be observed that the difference in power consumption for 4 bit and 8 bit resolution log tables is small in all the 4 cases. Since the log table is also hard-coded and synthesized inside the design module itself, the power estimate gives an overall view of the actual design. Considering 8 bit resolution log implementation, absolute detector based DRC with the smoothing stage consumes 58% more power compared to the one without the smoothing stage. Similarly, RMS detector based DRC with smoothing stage consumes 21% more power compared to without smoothing stage. Comparing the absolute detectors and RMS detectors, there is 67% increase in power consumption from absolute to RMS without smoothing stage and 28% increase when smoothing stage included. The synthesis report of the total number of standard cells for each architecture and the corresponding area are given in Table 3.



(a) Attack phase

(b) Release phase

Fig. 12. Error plots during transient period for attack and release phases. (Legends for Figs. 11 and 12 can be interpreted as follows: *Abs* - Absolute detector based DRC; *RMS* - RMS detector based DRC; *Sm* - DRC with smoothing stage included; *Log*4 - DRC implemented with 4 bit resolution logarithm table; *Log*8 - DRC implemented with 8 bit resolution logarithm table.).

5.2. Error analysis

The attack and release transient period of 81 samples are chosen for error analysis. The error plots are shown in Fig. 12. Error below 0.2 dB is not detectable by humans [13,18]. Minimum approximation errors (during attack phase), maximum approximation errors (during release phase) and Root Mean Square Error (RMSE) for the combined transient periods- attack and release phases are given in Table 5. After smoothing, the errors are less than 0.1 dB in all the cases. Considering the architectures without smoothing, maximum and RMSE are above 0.2 dB for 4 bit resolution log table. In the case of 8 bit resolution log table, the RMSE is around 0.1 dB and instantaneous errors go below 0.2 dB after initial few samples, which can be observed in Fig. 12. The layouts were not tested with different corners since we are making a relative comparison of power for different architectures and errors measured here are

Table 5
Final approximation errors estimated from output signal for the transient period of 81 samples for attack and release phase.

Error (dB)	Without smoothing				With smoothing			
	Abs		RMS		AbsSm		RMSSm	
	Log4	Log8	Log4	Log8	Log4	Log8	Log4	Log8
Min.(Att)	−0.753	−0.541	−0.753	−0.799	−0.110	−0.111	−0.113	−0.114
Max.(Rel)	0.747	0.117	0.396	0.124	0.125	0.122	0.119	0.122
RMSE	0.445	0.101	0.393	0.119	0.087	0.089	0.084	0.084

quantization errors due to logarithm table resolution which is independent of corner cases.

6. Conclusion

A new formula relating attack and release time parameters, envelope tracking decay coefficients and compression ratio parameters is proposed in this paper for the Dynamic Range Compression algorithm for hearing aid application. An absolute detector based and an RMS detector based feed-forward architectures with and without smoothing stages were implemented using 4 bit and 8 bit resolution LUT based logarithm at hardware level using UMC 65 nm standard cell libraries. The approximation errors and the post layout core power consumption were analyzed for the 8 different approaches and a relative comparison was done. The results show that the proposed techniques give accurate expected output at required time instants while conventional methods give erroneous output values. Hardware comparison shows that there is no significant difference in power consumption with an increase in log table resolution, while the approximation error reduces significantly. Smoothing stages can be included if a continuous gain transition is needed with the cost of increased power consumption. So we propose use of an absolute level detector based DRC without the smoothing stage for lowest power consumption and overall performance, using modified decay coefficient estimation techniques for a low power hearing aid design. In applications where high quality of sound is important, a smoothing filter can be incorporated at the output stage. Hardware implementation was carried out by standard Register Transfer Level procedures without incorporating any low power architectural optimizations. Hardware level implementations of different DRC architectures are rarely explored by the research community and hence, this paper can act as a basic platform for further optimizations at hardware level.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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