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Design and implementation of a signal processing ASIC for digital hearing aids

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ABSTRACT

People with hearing loss can be benefited from assistive devices like hearing aids. This article presents the implementation of a signal processing chip for digital hearing aid applications. The functionality of the proposed design was tested in real-time using two field programmable gate arrays (FPGAs), one of them modeled as a hearing aid processor and the other as an external audio CODEC. The hearing aid processor contains an 18-band 1/3-octave ANSI S1.11 filter bank, which performs the audiogram compensation and a dynamic range compression algorithm to restrict the output signal to an acceptable loudness. The functionality of an external audio CODEC was replicated in the other FPGA to act as the analog front end circuit of a hearing aid. Serial Peripheral Interface (SPI) was used for communication between the two FPGAs. The SPI protocol was modified to make the hearing aid programmable through the data in line of the interface itself. The proposed hearing aid chip was implemented using standard cell based design flow with a 5x5 mm fixed die size intended to fit in a 48-pin package.

1. Introduction

According to World Health Organization (WHO), 466 million people (more than 5% of the world's population; 432 million adults and 34 million children) are suffering from disabling hearing loss [1]. The majority of hearing impaired (HI) live in low and middle-income countries. WHO reports also project that 900 billion teenagers and young people are at risk of hearing loss due to the unsafe use of personal audio devices including smartphones and exposure to damaging levels of sound at noisy entertainment venues. Exposure to sounds in excess of 85 dB for 8 h and 100 dB for 15 min may lead to hearing impairment. The current production of hearing aids meets less than 10% of global need according to WHO. According to a survey by *The Hearing Review*, the average cost of a hearing aid per ear goes above $2000 [2]. So for a pair of hearing aids, the cost is not affordable for a person from a middle or low income group. We could not find a good comparative study on the price of hearing aid in Indian markets. The price of hearing aids can be reduced by a huge amount if it can be designed and manufactured locally. If a high-performance hearing aid, affordable by lower-income people can be developed, it would be a great achievement for healthcare in developing countries.

A digital hearing aid (DHA) is a complex real-time system capable of performing audio signal enhancement according to the requirements of a particular hearing loss. It consists of analog front end and digital signal processing blocks along with transducers. The basic block diagram of a DHA is shown in Fig. 1. The incoming sound signal is captured by the microphone and is given to an analog to digital converter (ADC). The digital output from the ADC is processed by the digital signal processor (DSP) and the processed signal is converted back to analog using a digital to analog converter (DAC) before sending it to the receiver.

The microphones for hearing aids need to have low power consumption, small size, low sensitivity to vibration and uniform frequency response over a range of 200 Hz to 5 kHz [3]. Receivers also have to be small in size and free from vibrations. An audio CODEC (Coder–Decoder) is composed of ADC and DAC. A CODEC can either be integrated into DSP or be used as a standalone chip. Low power consumption, small size, high dynamic range and high resolution are the main requirements of a CODEC for hearing aid application.

The fundamental concept of a hearing aid is to amplify the signal level in a particular frequency range where there is hearing loss as per the audiogram. In a DHA, the digital signal processing block does this function. A basic hearing aid DSP block consists of feedback cancellation (FBC), filter bank (FB), noise reduction (NR) and dynamic range compression (DRC) algorithms. Among these, filter bank and dynamic range compression algorithms are necessary in all the hearing aids, while FBC and NR are optional.

A patient having hearing loss has to go through a few steps before starting to use a hearing aid. An audiologist will measure the degree of

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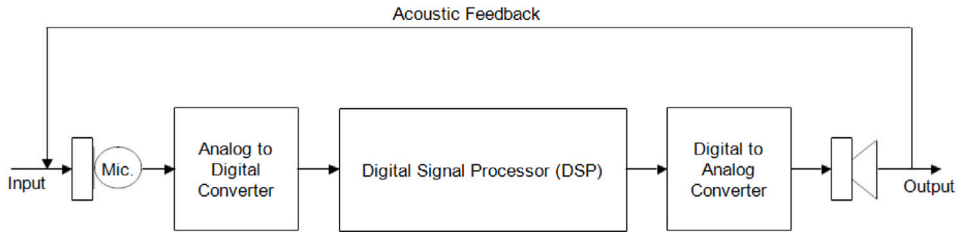


Fig. 1. DHA block diagram.

patient's hearing loss and decide the best possible solution after going through a set of standard procedures. The first step in fitting a hearing aid is to understand the severity of the loss. A hearing test will be carried out in a soundproof room with a calibrated audiometer, which can produce sounds at different frequencies at specified levels. The audiologist plays these sounds at very low intensities through a headphone. Then the intensity level is gradually increased until the sound becomes audible. The softest sounds heard by the subject at each frequency are recorded as the thresholds. Most hearing tests analyze sounds between 125 Hz and 8 kHz and from −10 dB to 120 dB Sound Pressure Level (SPL). From these recorded data, SPL v/s frequency graph, i.e., the audiogram is plotted. Based on the audiogram and the patient's choice, the audiologist chooses a particular hearing aid and does the initial fitting according to the gain curves obtained from any of the available gain prescription formulas. The most common methods available for hearing aid gain prescription are: NAL-RP (National Acoustic Laboratory-Revised Profound), NAL-NL1(Non-Linear 1), NAL-NL2(Non-Linear 2) and DSL I/O(Desired Sensation Level Input/Output) [4]. After the initial fitting, fine-tuning is done by adjusting the gain in each band manually, considering patient feed-back.

If a patient fitted with a hearing aid feels that there is no advantage in wearing a hearing aid or if it causes any other adverse side effects, the person may stop using it. It is necessary to understand and solve the major reasons why patients stop using hearing aids. In a study by McCormack et al., the authors have collected most of the available data on user satisfaction via a scoping study [5]. Out of those, they have selected 10 articles reporting reasons for non-use of hearing aids and found a number of reasons including hearing aid value, fit and comfort, maintenance of the hearing aid, attitude, device factors, financial reasons, psychosocial/situational factors, healthcare professionals' attitudes, ear problems and appearance. The most important issue was the hearing aid value, i.e., the hearing aid did not provide enough benefit and comfort to the hearing impaired. Another important conclusion was, the stigma of wearing hearing aids had minimal impact on discontinuation.

A hearing aid can be considered as one of the most challenging applications when it comes to IC design because of its real-time processing and stringent low power requirement. For hearing aid designers, there can be three primary challenges [6]: high performance (in terms of sound quality and computational capability), low power consumption (a battery current drain ≤ 1 mA) with limited supply voltage (approximately 1 V) and small physical size (depending on the style). Since all three are interrelated, it is the task of the designer to find a trade-off between these challenges. There are different options in the case of hardware platforms available to implement the signal processing algorithms for hearing aids. For testing the algorithm in real-time during the initial stages of the design, it is a common practice to use low power general-purpose digital signal processors. Because of its size and comparatively higher power consumption, it is difficult to consider these processors for hearing aid products other than body worn type. Field Programmable Gate Arrays (FPGAs) are another option available for testing the algorithms in real-time. Application Specific Integrated Circuits (ASICs) with custom-designed dedicated architectures for the particular signal processing techniques are the best way to realize the algorithms in hardware. Various hearing aid implementations available in the literature are based on one of these hardware platforms [7–27].

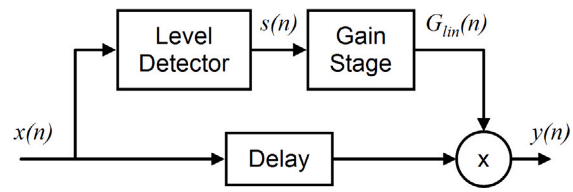


Fig. 2. Block diagram of a feed-forward DRC algorithm.

The performance of the hearing aids is largely limited by the current battery technology. Even though rechargeable batteries are available, 1.3 V zinc-air batteries are used in most of the hearing aids. To get a reasonable battery life (at least greater than 50 h [24], the current consumption should be minimum. All the hearing aid ASIC implementations gave at most care to keep the power consumption in the acceptable range of around 1 mW as specified in WHO guidelines [28]. The power consumption also increases with the complexity of various algorithms incorporated in different implementations. Since each of the designs includes different levels of functionality and manufactured with different technology nodes, a direct comparison of power is not possible between them. Some of the implementations show that voltage scaling works well in reducing power consumption, [23,24]. Wei et al. [23], reported that the power consumption of the design got reduced from 1.09 mW to 0.314 mW when the supply voltage was reduced from 1 V to 0.6 V. The chip size depends on the complexity of the algorithm and the technology node used for fabrication. A chip area less than 25 mm^2 may be enough for Behind the Ear (BTE) and In the Ear (ITE) devices [24]. The frequency range of the hearing aids is mainly limited by the microphone and receiver characteristics. ANSI S3.22 standard specifies a minimum frequency range of 200 Hz to 5 kHz [3]. The audiogram gives information only up to 8 kHz. So a sampling frequency above 16 kHz may work well for the hearing aids. As the sampling frequency increases, the dynamic power consumption also increases.

For lip synchronicity, a delay less than 70 ms is sufficient [29] which is easily attainable with the current algorithms. But the major problem with delay is the comb filter effect, which occurs when the delayed sound that comes through the hearing aid combines with the sound directly coming through the vent or bone conduction. Even a delay of 3 ms may create an echo. For a delay higher than 10 ms, this effect becomes significant and affects the intelligibility. So hearing aid delay is a major factor in the design and needs to be kept as small as possible. In most of the literature reporting chip implementations, the delay of the design is not mentioned and hence it is very difficult to compare the actual performance of different designs. Park et al. [15], reported a delay of 10.9 ms. The other delays mentioned, 19.4 ms by [14] and 32 ms by [23] are higher than the acceptable delay for a smooth output from a hearing aid.

In every hearing aid design, the frequency decomposition algorithms are required to perform the auditory compensation and amplitude compression is needed to restrict the sound intensity to an acceptable loudness to protect the hearing aid wearers from further

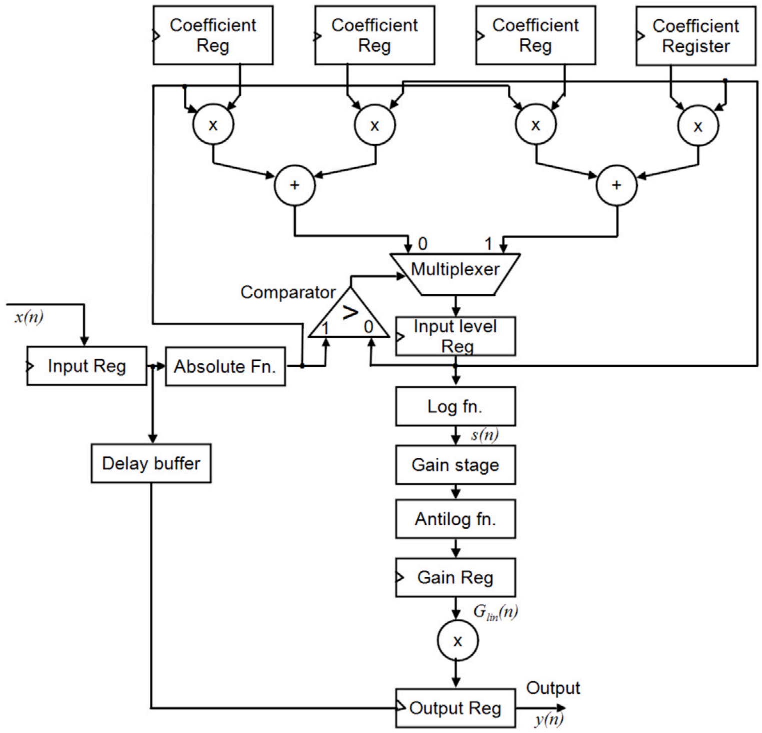


Fig. 3. Hardware architecture of the DRC algorithm.

damage to their residual hearing. Initial hearing aid systems were based entirely on analog technology [8,10,12,21]. In these designs, the frequency decomposition was achieved mainly by tunable switched-capacitor filters [10,12]. The automatic gain control (AGC) circuits perform the functionality of Dynamic Range Compression (DRC). When the designs started migrating from analog to digital, the implementations were mainly based on general-purpose DSP platforms [9,13, 14,17]. Later, dedicated ASIC designs started replacing the digital hearing aid implementations. A direct comparison of these different implementations is not possible as each design depends on so many factors with its own characteristics.

In earlier days, hard limiters were used to restrict the output from going beyond a tolerable loudness [7,9]. In hard limiters, the output was clipped if it goes beyond a particular threshold. Later, non-linear compression techniques were introduced. Magotra et al. implemented the compression curve using approximation techniques like the Taylor series method in the linear domain [30]. In the current state of the art hearing aids, the compression is applied in the log domain after converting the estimated input signal to the log domain [31,32] so that the non-linear compression curve becomes a piece-wise linear curve.

For any hearing aid, the most power consuming part is the filter bank architecture. The ability of a hearing aid with which it can fit the prescription gain to compensate for the loss corresponding to each frequency in a patient's audiogram is decided by the frequency resolution of the filter bank. This resolution depends on the number of bands and the filter bank structure. The power consumption as well as the delay of the hearing aid are dependent on the individual filter orders, type of filtering and the number of bands present in the filter bank architecture. In digital domain, uniform filter banks were used in earlier implementations [13,15]. Non-uniform structures started replacing the uniform structures in recent implementations [27,33,34]. Mainly the introduction of widely accepted non-linear gain prescription formulas which give the compensation gains in an 18-band non-uniform manner (NAL-NL1, NAL-NL2 and DSL I/O) and the requirement of lesser number of bands to match that frequency distribution motivated the use of non-uniform filter banks. Even though recent implementations use these advanced non-uniform structures, detailed analysis of the delay and the feasibility of those systems on real hardware [23,24,26,27,35] are not provided.

In this paper, the implementation of a signal processing application specific integrated circuit (ASIC) for digital hearing aids is presented. The design contains an 18-band filter bank and dynamic range compression algorithms. The compression algorithm proposed by Deepu et al. [36] is used with an 8-bit resolution look-up table based logarithm implementation without incorporating the smoothing stage. The 18-band 1/3-octave ANSI S1.11 filter bank based on Interpolated Finite Impulse Response (IFIR) technique proposed by Deepu et al., is used for frequency decomposition [37]. The chip contains a serial peripheral interface (SPI) to communicate with the external audio CODEC and can be programmed using the same interface. The functionality of the proposed design was tested in real-time using two FPGA development boards. The paper is organized as follows. Section 2 gives a brief explanation of the algorithms used for the design. Details of the real-time testing using two FPGAs are explained in Section 3. The ASIC design using Semiconductor Laboratory (SCL) 180 nm standard cell PDK is given in Section 4. The conclusions are drawn in Section 5.

2. Algorithm description

The proposed hearing aid ASIC contains a dynamic range compression algorithm and an 18-band filter bank algorithm.

2.1. Dynamic range compression algorithm

In this design, an absolute detector based DRC without smoothing stage is used as shown in Fig. 2 It has a level detection stage and a gain stage. The incoming signal level is continuously monitored by the level detection stage and the compression is applied at gain stage depending on the measured input level. In absolute detector based DRC, the absolute value of the input signal is measured over a small duration using an envelope detecting recursive filter. If the input goes beyond a particular threshold value (Compression Threshold, CT), the output needs to be compressed according to a compression curve obtained from the gain

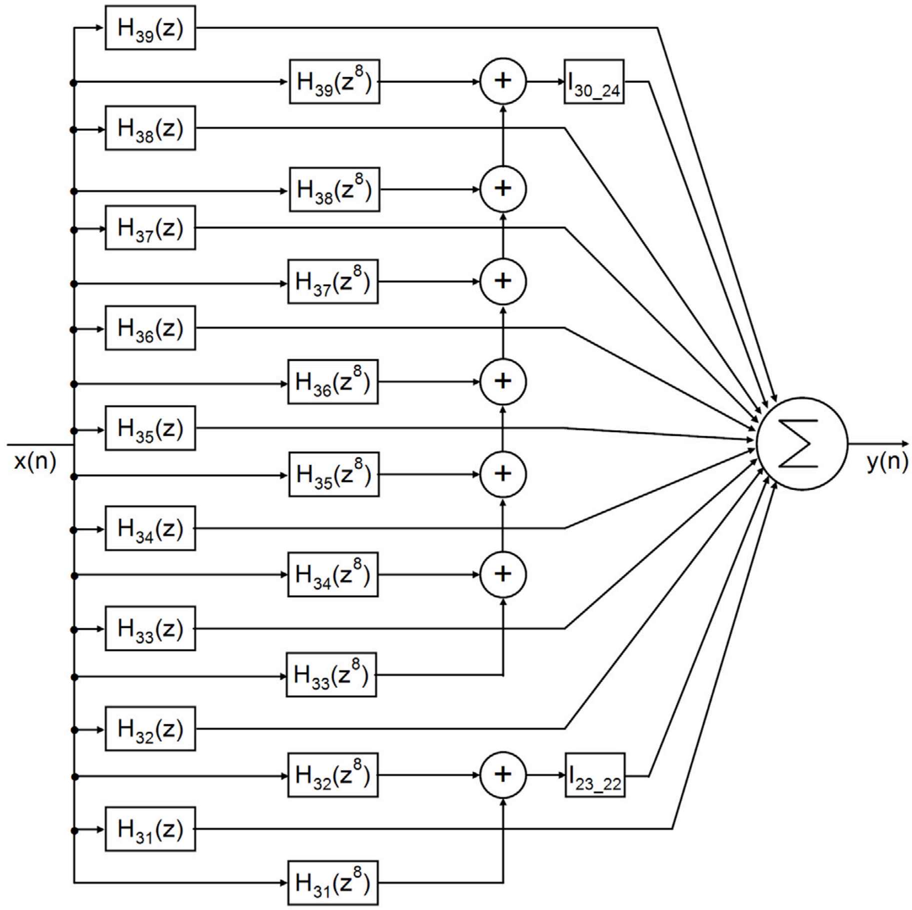


Fig. 4. The 18-band ANSI S1.11 filter bank structure used for the implementation [37].

prescription procedures [36]. Since it is a non-linear operation, the compression is applied after converting the measured input level to the log domain $s(n)$, to make the hardware implementation easier. In Fig. 2, $x(n)$ is the input signal, $y(n)$ is the output signal and $G_{lin}(n)$ represents the compression gain after applying the antilogarithm function.

The hardware implementation was carried out using Verilog Hardware Description Language (HDL). All the inputs and parameters were represented in signed 16-bit fixed point format. An 8-bit resolution look-up table was used for logarithm and antilogarithm implementations. The input signal $x(n)$ is passed through a register array before multiplying with the compression gain factor to compensate for the latency introduced by the various pipeline registers used at the implementation stage. The hardware architecture of the implemented DRC is shown in Fig. 3. In the hardware architecture, the coefficient registers are used to store the attack and release phase decay coefficients. These parameters decide how fast the compression should be applied and released back to the normal signal level.

2.2. Filter bank algorithm

The hearing aids should be able to match the gain curves obtained from the prescription procedures corresponding to different audiograms. The filter bank architecture proposed by Deepu et al. [37] gives an acceptable audiogram matching performance for the gain prescription procedure, National Acoustic Laboratory - Non-Linear 2 (NAL-NL2) and comparatively easier to implement on hardware with lesser power consumption. The filter bank reports a group delay of 9.75 ms. Since the entire filter bank is running on the same sampling frequency, it would be easier to incorporate further multi-band signal enhancement algorithms to the hearing aid in the future. The architecture of the filter bank is shown in Fig. 4. It has 18 analysis filters and two interpolation filters. The upper nine bands of the filter bank ($H_{39}(z)$ to $H_{31}(z)$) are designed using Parks–McClellan (PM) algorithm and lower nine bands ($H_{30}(z)$ to $H_{22}(z)$) were derived from upper nine bands by interpolating by a factor of 8 ($H_{39}(z^8)$ to $H_{31}(z^8)$). The interpolation filters, I_{30_24} and I_{23_22} were used to cancel out the image frequencies due to interpolation [38].

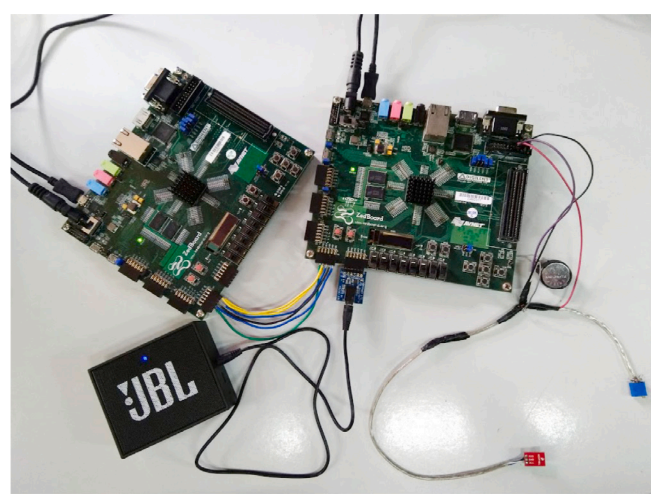


Fig. 5. Real-time testing setup of the hearing aid system using two FPGA development kits.

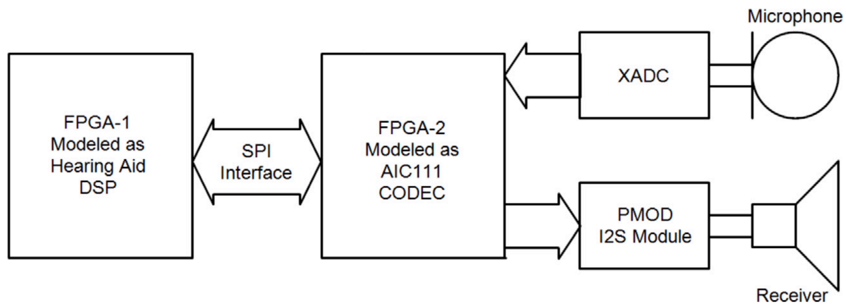


Fig. 6. Top level block diagram of the experimental setup.

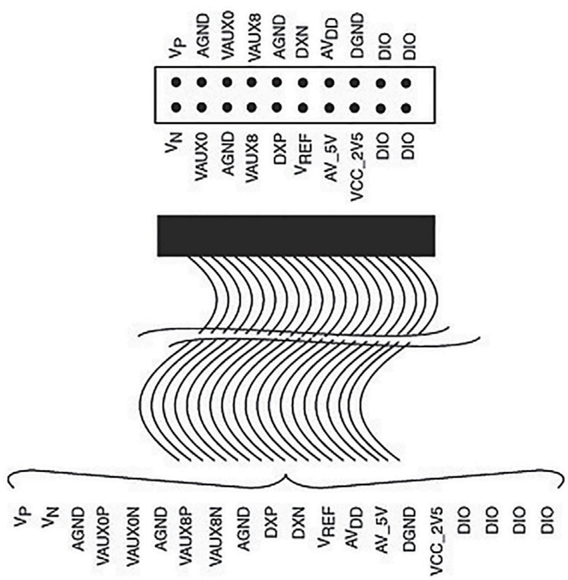


Fig. 7. Agile Mixed Signaling (AMS) connector pin out diagram of the ZedBoard [39].

A multi-MAC (Multiply-Accumulate) based methodology was adopted for the hardware implementation to reduce power consumption. The sampling frequency was chosen as 24 kHz. The clock frequency of 384 kHz was used for each multiplication operation. It supports 15 multiplications per MAC for the chosen sampling frequency. Therefore, a total of 30 MAC units are needed for the entire filter bank implementation.

3. FPGA implementation and real-time testing

The proposed hearing aid architecture with 18-band ANSI S1.11 filter bank and dynamic range compression algorithms was implemented and tested in real-time using two FPGA development kits as shown in Fig. 5. Two Digilent ZedBoards™ having Xilinx® Zynq-7000 SoC were used for the experiment [39]. ZedBoard has 85 000 programmable logic elements along with an ARM® Cortex-A9 dual-core processor. The available programmable logic elements were enough to meet our design requirement. The FPGA part of the kit has a 100 MHz clock source which meets the master clock requirement of 6.144 MHz of the design. The proposed hearing aid DSP was implemented on one of the ZedBoards. The other ZedBoard was modeled as an external audio CODEC.

Texas Instruments (TI) has a 1.3 V micro-power voice band audio CODEC chip, AIC111, specifically designed for low power audio processing applications like hearing aids [40]. It is a single channel CODEC with delta-sigma ADC and DAC technology having a frequency response from 100 Hz to 10 kHz. The chip has a typical current drain of 350 μA. The ADC gives a 16-bit digital output and the DAC is capable of converting 16–24 bits digital data to an analog signal. AIC111 can be interfaced with external DSPs either through McBSPDSP-Codec Interface (SACI) protocol or through Serial Peripheral Interface (SPI) protocol. SACI is generally used for interfacing with TI DSPs and SPI for other devices. The slave devices need to have a compatible SPI slave protocol to communicate with AIC111. Therefore, in our hearing aid DSP, an SPI slave protocol was added to communicate with the external CODEC.

Instead of using the AIC111 breakout board to test the design, a second FPGA development board was modeled to replicate the functionality of the audio CODEC. This second FPGA test setup can be used without much modifications to test the fabricated chip in the future. The top-level block diagram of the experimental setup is shown in Fig. 6. An omni-directional MEMS microphone, ADMP401, having a flat frequency response from 100 Hz to 15 kHz was used for our experiment [41]. The analog audio signal from the external microphone was converted to the digital domain using the XADC present in the ZedBoard. The ZedBoard has two channels of analog to digital converters embedded in it. The pinout diagram of the Agile Mixed Signaling (AMS) header of the ZedBoard is shown in Fig. 7 [39]. The XADC channel-8 is used for the experiment [42]. It is a 12-bit, 1-MSPS (Mega Samples Per Second) ADC with 1 V peak to peak input level. The 12-bit data from ADC is internally converted to 16 bits by extending the LSB to extra four bits. The ADC was configured in single-channel bipolar mode for our experiment.

Digilent pmod I^2S module having a 24-bit digital to analog converter (DAC) is used to convert the processed signal back to the analog domain and play the output through the standard stereo audio port [43]. The DAC accepts 16-24 bit data input. It uses Integrated Interchip Sound (I^2S) protocol for communication with host board GPIO ports. The module has four signals namely, Master Clock ($MCLK$), Left–right Clock ($LRCK$), Serial Clock (SCK) and Serial Data Input ($SDIN$) along with supply pins VDD and GND. $LRCK$ is used to send data to the left and right channels. Each channel is chosen by ON and OFF periods of the $LRCK$. Therefore $LRCK$ needs to be equivalent to the sampling frequency, which is 24 kHz. The data serializing clock, SCK needs to run at two times of 16-bits, to send 16-bit data to one of the channels. Hence SCK is set as 768 kHz. The $MCLK/LRCK$ ratio was chosen as 256 from the data sheet according to our requirement, which gives a master clock ($MCLK$) frequency of 6.144 MHz. The timing diagram of the protocol is shown in Fig. 8.

The interfacing used for communication between the two FPGAs is shown in Fig. 9. The SPI master protocol of AIC111 was replicated in the CODEC FPGA with a few modifications to make the hearing aid ASIC programmable. The hearing aid FPGA was modeled as an SPI slave and the CODEC FPGA was modeled as an SPI master. It has mainly four signals, data in line to the slave - $mosi$ (Master Out Slave In), data out line from the slave - $miso$ (Master In Slave Out), the serial clock, $sclk$, and a synchronization signal $frame$. An extra control signal (p_d_ctrl) is added to the protocol in addition to the AIC111 SPI standard, to transfer the programmable parameters also through the same serial data in port

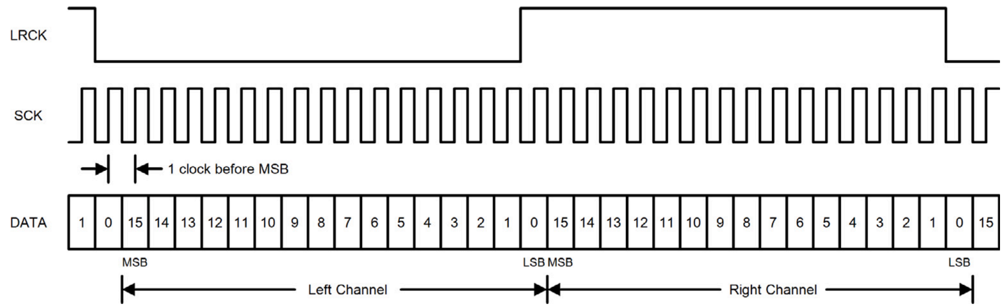


Fig. 8. Timing diagram of I^{2}S interface.

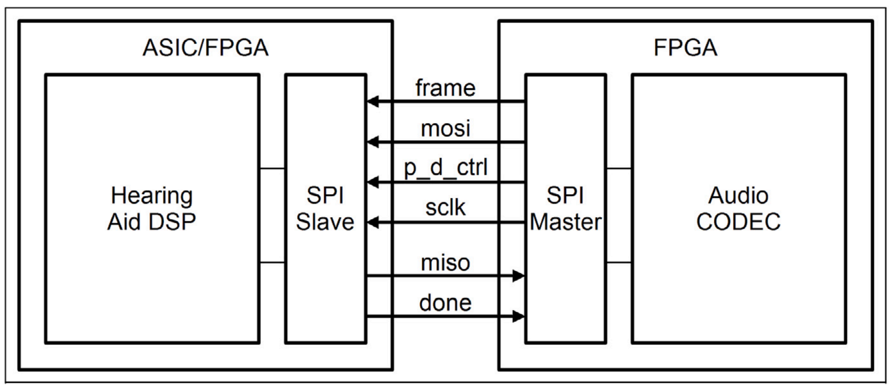


Fig. 9. SPI interface between two FPGAs.

of the interface. In AIC111, the protocol is defined in such a way that it can send up to 24-bit data in a single frame. An idle period of 8 cycles is given for stable data capture. The serial clock is designed to support this 24-bit frame size with eight extra cycles kept as idle. The control pulse $frame$ is used to capture the data during the idle period of $sclk$. Since the sampling frequency is set as 24 kHz, the serial clock is chosen as 384 kHz, i.e., 32 times the sampling frequency. A master clock, $mclk$ of 6.144 MHz is used to generate the SPI signals which matches the master clock frequency used for the PMOD I^{2}S module.

The timing diagrams used for SPI communication are shown in Figs. 10 and 11. The hearing aid programmable parameters, i.e., prescribed gains for filter bank and the coefficients for DRC are sent initially through the data in line by keeping p_d_ctrl signal $high$ as shown in Fig. 10. In the 24-bit data frame, the 16-bit parameters are followed by a 5-bit register address of each parameter. The remaining 3-bits are do not care. These parameters were stored in the block memory of CODEC FPGA. Once all the parameters are transferred, the p_d_ctrl signal goes low and audio data transfer starts as shown in Fig. 11. Since we are using 16-bit data, 8-bits are not used in both $mosi$ and $miso$ in each frame.

4. ASIC implementation

The proposed hearing aid signal processing architecture was implemented using Semi-Conductor Laboratory (SCL) 180 nm Process Design Kit (PDK) as they support free fabrication of the chip for academic purposes. The module hierarchy of the ASIC is shown in Fig. 12. The top module, $top\_chip\_wrapper$ has 12 pins including the power supply pins $vdd, vss, vddo$ and $vsso$ for the core and the pads respectively. $mclk$ is the master clock (6.144 MHz) pin and rst is the asynchronous master reset pin. The clock signals other than the SPI serial clock, $sclk$ are generated from the master clock inside the $spi\_slave\_wrapper$ module. Both the audio data as well as the control parameters for the filter bank and DRC are transferred to the hearing aid through the serial data in pin of the SPI slave, $mosi$. This data transfer is initialized and synchronized using an extra $start$ signal added to the SPI master module. The control parameters, i.e., the insertion gain values for each of the 18 bands in the filter bank, and the DRC control signals such as, attack and release time coefficients, compression ratio and the threshold are separately mapped to the filter bank and DRC modules through intermediate signal lines $param\_in$ and $param\_addr$ as shown in Fig. 12.

A fixed die size of 5 × 5 mm with 48 pin package was chosen for the design as SCL supports limited options for academic purposes. Two sets of power pads, i.e., four pads for core power and ground pins (2 vdd and 2 vss pads) and one set of pads for I/O pad supply (1 $vddo$ and 1 $vsso$ pads) were used on all four sides. Out of the remaining 16 pins available, 8 pins were kept as dummy pins and eight pins were assigned for controlling the functionality externally and testing the intermediate stages of the chip. For the implementation of the ASIC, the SCL preferred EDA tool flow was followed. The RTL was written using Verilog HDL, after verifying the algorithms in MATLAB®. The design was synthesized using Synopsys Design Compiler®. The synthesis delay constraints were decided based on the different clock frequencies and the load information available from the datasheet of AIC111 audio CODEC. The physical design was carried out using Synopsys IC Compiler®. After verifying the gate-level simulation (GLS), the physical verification was done in Cadence Virtuoso and Calibre® tool from Mentor Graphics. The layout of the proposed hearing aid ASIC is shown in Fig. 13. The layout was clean with Design Rule Check (DRC), Antenna and Layout v/s Schematic (LVS) verification checks with the rule files provided by the foundry. It can be observed that the 48 pads were distributed equally between all 4 sides with 12 pads per each side. SCL supports 4 metal layers and we used all 4 metals for routing and top metals, metal 3 and metal 4 for power routing.

The proposed implementation was verified with different audiograms available in [44]. State of the art clinical fitting procedure, NAL-NL2 was used for testing the algorithm. Even though the subjective evaluation is not done, the objective results from the post-layout simulation of the implementation meet the delay (less than 10 ms) and the matching error (less than 1 dB) performance requirements.

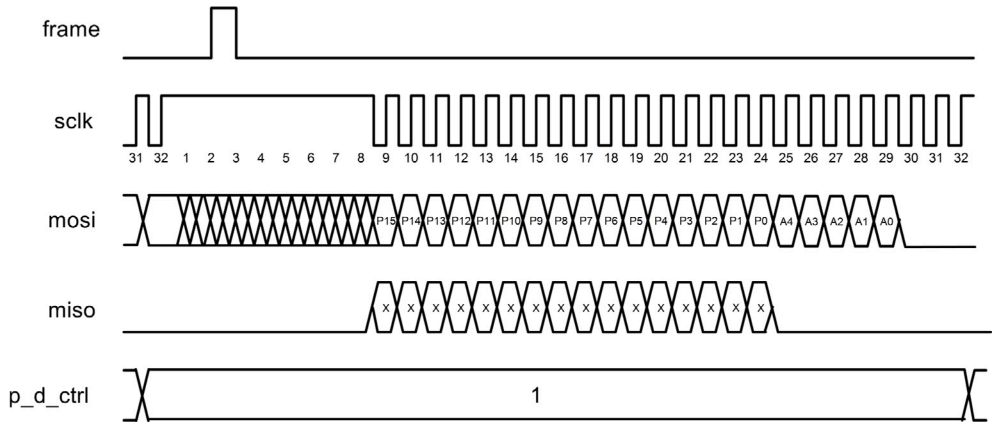


Fig. 10. SPI protocol with $p\_d\_ctrl = 1$.

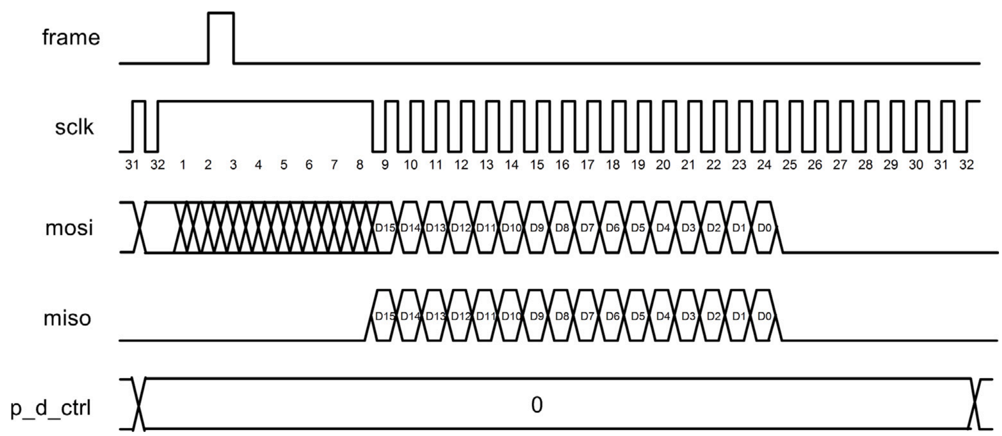


Fig. 11. SPI protocol with $p\_d\_ctrl = 0$.

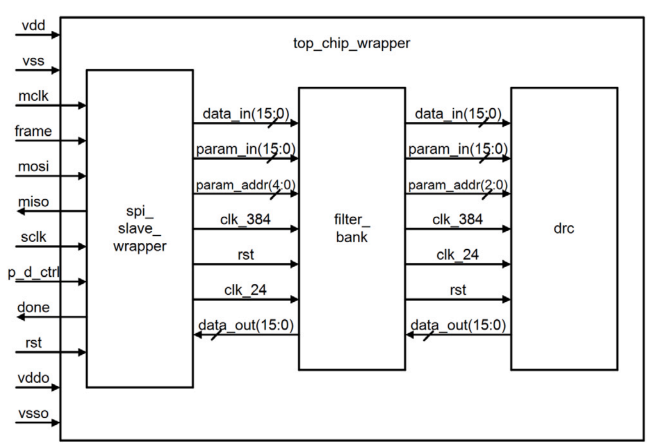


Fig. 12. Hearing aid module hierarchy.

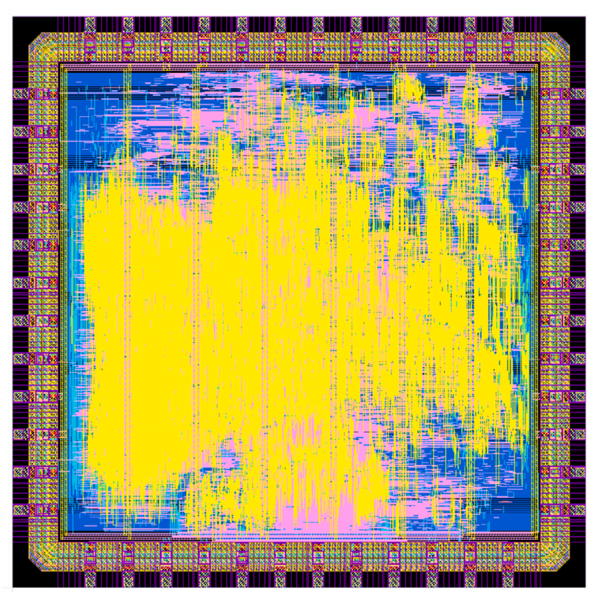
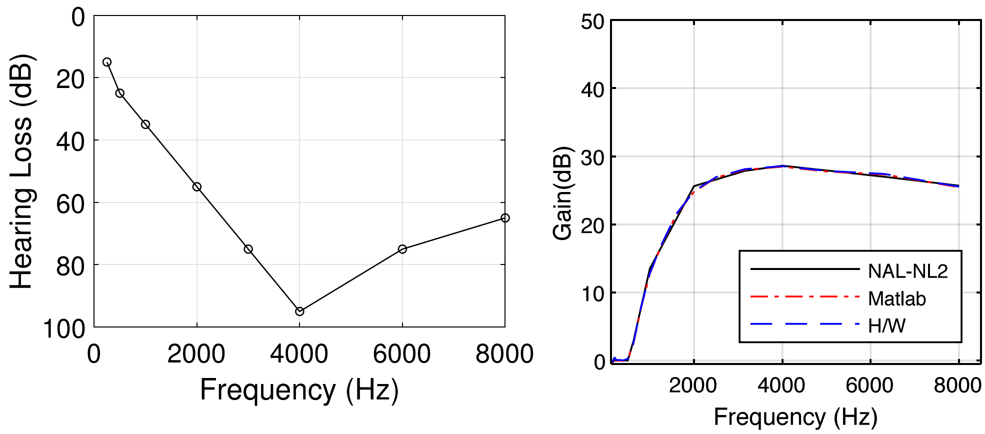


Fig. 13. Complete hearing aid ASIC layout using SCL 180 nm.

A sample audiogram and its matching results for NAL-NL2 prescription from MATLAB and hardware implementation simulations are shown in Fig. 14. The audiogram was obtained from [44]. The layout simulations were done using a test sequence consisting of the sinusoids of the 18 center frequencies of the filter bank. All 8 test audiograms from [44] were tested using the post layout netlist and the audiogram matching error results were within 1 dB as in [37]. Finally, the functionality was tested in real-time using the two FPGA system based test setup.

5. Conclusion

An ASIC design and real-time testing details of a signal processing architecture for digital hearing aids are presented in this paper. The



(a) A sample audiogram [44] (b) Matching results

Fig. 14. NAL-NL2 prescription and the matching results obtained from Matlab and hardware implementations for a sample audiogram.

chip was designed in such a way that it is programmable externally through the SPI interface. SCL 180 nm PDK was used for the ASIC design. Two ZedBoards were used for testing the design in real-time. The audio signal was recorded using an external microphone and converted to digital using the XADC present in ZedBoard. Data transfer between two FPGAs were performed using SPI protocol. The processed data was converted to analog using a PMOD I^2S module.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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References

[1] WHO, Deafness and hearing loss, 2019, [Online; accessed 7-February-2020] https://www.who.int/news-room/fact-sheets/detail/deafness-and-hearing-loss.
[2] K.E. Strom, HR 2013 hearing aid dispenser survey: dispensing in the age of internet and big box retailers, Hear. Rev. (2014) April 8.
[3] S3 ANSI, 22–2003 Specification of Hearing Aid Characteristics, Standard S3.22, ANSI, 2003.
[4] E.E. Johnson, Same or different: Comparing the latest NAL and DSL prescriptive targets, Audiology (2012) Online: 20Q Monthly Featured Article.
[5] A. McCormack, H. Fortnum, Why do people fitted with hearing aids not wear them? Int. J. Audiol. 52 (5) (2013) 360–368.
[6] OnSemiconductor, TND 6092 / D solving the hearing aid platform puzzle seven things hearing aid manufacturers should think about, 2014.
[7] R. Morley, G.L. Engel, T.J. Sullivan, S.M. Natarajan, VLSI based design of a battery-operated digital hearing aid, in: ICASSP-88., International Conference on Acoustics, Speech, and Signal Processing, IEEE, 1988, pp. 2512–2515.
[8] F. Callias, F.H. Salchli, D. Girard, A set of four ICs in CMOS technology for a programmable hearing aid, IEEE J. Solid-State Circuits 24 (2) (1989) 301–312.
[9] L.B. Nielsen, A computer controlled digital master hearing aid, in: IEEE International Symposium on Circuits and Systems, IEEE, 1989, pp. 1291–1294.
[10] D. Wayne, M. Rives, T.H.T. Huynh, D. Preves, J. Newton, A single-chip hearing aid with one volt switched capacitor filters, in: 1992 Proceedings of the IEEE Custom Integrated Circuits Conference, IEEE, 1992, pp. 5–7.
[11] J. Svean, A. Krokstad, S. Sorsdal, An all digital concha hearing aid, in: Proceedings of IEEE Workshop on Applications of Signal Processing to Audio and Acoustics, IEEE, 1993, pp. 85–88.
[12] A. Bhattacharyya, R.S. Rana, S. Guha, R. Bahl, R. Anand, M. Zarabi, P. Govindacharyulu, U. Gupta, V. Mohan, J. Roy, et al., A micropower analog hearing aid on low voltage CMOS digital process, in: Proceedings of 9th International Conference on VLSI Design, IEEE, 1996, pp. 85–89.
[13] H. McAllister, N. Black, N. Waterman, A body worn digital hearing aid, in: Engineering in Medicine and Biology Society, 1995., IEEE 17th Annual Conference, Vol. 2, IEEE, 1995, pp. 1613–1614.
[14] J. Tejero, S. Bernal, J. Hidaldo, J. Fernandez, R. Urquiza, A. Gago, A digital hearing aid that compensates loudness for sensorineural hearing impairments, in: 1995 International Conference on Acoustics, Speech, and Signal Processing, Vol. 5, IEEE, 1995, pp. 2991–2994.
[15] Y.C. Park, D.W. Kim, W.K. Kim, S.i. Park, A digital hearing aid with 8-band curvilinear loudness fitting, in: ISCE'97. Proceedings of 1997 IEEE International Symposium on Consumer Electronics (Cat. No. 97TH8348), IEEE, 1997, pp. 39–42.
[16] H. Neuteboom, B.M. Kup, M. Janssens, A DSP-based hearing instrument IC, IEEE J. Solid-State Circuits 32 (11) (1997) 1790–1806.
[17] T. Stetzler, N. Magotra, P. Gelabert, P. Kasthuri, S. Bangalore, Low power real-time programmable DSP development platform for digital hearing aids, in: 1999 IEEE International Conference on Acoustics, Speech, and Signal Processing. Proceedings. ICASSP99 (Cat. No. 99CH36258), Vol. 4, IEEE, 1999, pp. 2339–2342.
[18] P. Mosch, G. van Oerle, S. Menzl, N. Rougnon Glasson, K. Van Nieuwenhove, M. Wezelenburg, A 660-/spl mu/W 50-Mops 1-V DSP for a hearing aid chip set, IEEE J. Solid-State Circuits 35 (11) (2000) 1705–1712.
[19] O. Paker, J. Sparso, N. Haandbæ k, M. Isager, L.S. Nielsen, A heterogeneous multiprocessor architecture for low-power audio signal processing applications, in: Proceedings IEEE Computer Society Workshop on VLSI 2001. Emerging Technologies for VLSI Systems, IEEE, 2001, pp. 47–53.
[20] D.G. Gata, W. Sjursen, J.R. Hochschild, J.W. Fattaruso, L. Fang, G.R. Iannelli, Z. Jiang, C.M. Branch, J.A. Holmes, M.L. Skorcz, E.M. Petilli, S. Chen, G. Wakeman, D.A. Preves, W.A. Severin, A 1.1-V 270-/spl mu/A mixed-signal hearing aid chip, IEEE J. Solid-State Circuits 37 (12) (2002) 1670–1678.
[21] F. Serra Graells, L. Gomez, J.L. Huertas, A true-1-V 300-/spl mu/W CMOS-subthreshold log-domain hearing-aid-on-chip, IEEE J. Solid-State Circuits 39 (8) (2004) 1271–1281.
[22] S.J. Lee, S. Kim, H.J. Yoo, A low power digital signal processor with adaptive band activation for digital hearing aid chip, in: 2007 IEEE International Symposium on Circuits and Systems, IEEE, 2007, pp. 2730–2733.
[23] C.W. Wei, Y.T. Kuo, K.C. Chang, C.C. Tsai, J.Y. Lin, Y. FanJiang, M.H. Tu, C.W. Liu, T.S. Chang, S.J. Jou, A low-power mandarin-specific hearing aid chip, in: 2010 IEEE Asian Solid-State Circuits Conference, IEEE, 2010, pp. 1–4.
[24] P. Qiao, H. Corporaal, M. Lindwer, A 0.964 mW digital hearing aid system, in: 2011 Design, Automation & Test in Europe, IEEE, 2011, pp. 1–4.
[25] Y. Ku, J. Sohn, J. Han, Y. Baek, D. Kim, A high performance hearing aid system with fully programmable ultra low power DSP, in: 2013 IEEE International Conference on Consumer Electronics (ICCE), IEEE, 2013, pp. 352–353.
[26] K.C. Chang, S.C. Luo, C.J. Huang, C.W. Liu, Y.H. Chu, S.J. Jou, An ultra-low voltage hearing aid chip using variable-latency design technique, in: 2014 IEEE International Symposium on Circuits and Systems (ISCAS), IEEE, 2014, pp. 2543–2546.
[27] L.M. Chen, Z.H. Yu, C.Y. Chen, X.Y. Hu, J. Fan, J. Yang, Y. Hei, A 1-V, 1.2-mA fully integrated SoC for digital hearing aids, Microelectron. J. 46 (1) (2015) 12–19.
[28] WHO, Guidelines for Hearing Aids and Services for Developing Countries, Tech. Rep., World Health Organisation, 2004.
[29] R.W. Bauml, W. Sorgel, Uniform polyphase filter banks for use in hearing aids: design and constraints, in: Signal Processing Conference, 2008 16th European, IEEE, 2008, pp. 1–5.

[30] N. Magotra, P. Kasthuri, Y. Yang, R. Whitman, F. Livingston, Multichannel adaptive noise reduction in digital hearing aids, in: ISCAS'98. Proceedings of the 1998 IEEE International Symposium on Circuits and Systems (Cat. No. 98CH36187), Vol. 6, IEEE, 1998, pp. 582–585.

[31] K.C. Chang, Y.T. Kuo, T.J. Lin, C.W. Liu, Complexity-effective dynamic range compression for digital hearing aids, in: Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on, IEEE, 2010, pp. 2378–2381.

[32] J.M. Kates, Principles of digital dynamic-range compression, Trends Amplif. 9 (2) (2005) 45–76.

[33] Y.T. Kuo, T.J. Lin, Y.T. Li, C.W. Liu, Design and implementation of low-power ANSI S1. 11 filter bank for digital hearing aids, IEEE Trans. Circuits Syst. I. Regul. Pap. 57 (7) (2010) 1684–1696.

[34] C.W. Liu, K.C. Chang, M.H. Chuang, C.H. Lin, 10-Ms 18-band quasi-ANSI S1. 11 1/3-Octave filter bank for digital hearing aids, IEEE Trans. Circuits Syst. I. Regul. Pap. 60 (3) (2013) 638–649.

[35] V. Purushothaman, R. Ramadevi, Performance enhancement in digital hearing aidsystems using tunable filter, Microprocess. Microsyst. 79 (2020) 103294.

[36] S.P. Deepu, R. Kini, D.S. Sumam, Accurate estimation of decay coefficients for dynamic range compressors in hearing aids and a hardware level comparison of different architectures, Microprocess. Microsyst. 74 (2020) 102967.

[37] S.P. Deepu, R. Kini, D.S. Sumam, 18 Band ANSI S1. 11 filter bank based on interpolated finite impulse response technique for hearing aids, J. Eng. 2020 (9) (2020) 760–767.

[38] P.P. Vaidyanathan, Multirate Systems and Filter Banks, Pearson Education India, 1993.

[39] ZedBoard, ZedBoard Zynq-7000 development board reference manual, 2014, [Online; accessed 11-February-2020] https://reference.digilentinc.com/reference/programmable-logic/zedboard/reference-manual.

[40] TI, IC design specification 1.3-V MicroPower DSP/uC voice band audio codec, 2005, [Online; accessed 06-October-2019] https://www.ti.com/lit/ds/symlink/aic111.pdf.

[41] A. Devices, Omnidirectional microphone with bottom port and analog output, 2012, [Online; accessed 18-February-2020] https://www.analog.com/media/en/technical-documentation/obsolete-data-sheets/ADMP401.pdf.

[42] Xilinx, 7 series FPGAs and zynq-7000 SoC XADC dual 12-bit 1 MSPS analog-to-digital converter user guide, 2018, [Online; accessed 25-October-2019] https://www.xilinx.com/support/documentation/user_guides/ug480_7Series_XADC.pdf.

[43] Digilent, Pmod I2S reference manual, 2016, [Online; accessed 16-November-2019] https://reference.digilentinc.com/reference/pmod/pmodi2s/reference-manual.

[44] Earinfo, How to read your hearing test, 2014, [Online; accessed 16-May-2019] http://www.earinfo.com/how-to-read-a-hearing-aid-test/common-audiograms.

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