

Adapting Pettigrew's Amplitude-locked loop for Fast and Synchronized Extraction of Fundamental and Harmonics

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Abstract—The separation of the fundamental from a distorted waveform is an important component in the implementation of a custom power device. A novel scheme for synchronous extraction of harmonics/fundamental in a distorted periodic waveform is described here. An intuitive explanation is provided for the operation of the algorithm focusing on the process of amplitude locking and filtering capability. Performance aspects are analysed and discussed. The design parameters are identified and their influence on the performance parameters are identified. A means for choosing design parameters to achieve the optimum performance is provided. Main features of the proposed scheme are its simplicity, excellent insensitivity to harmonics, noise rejection, availability of both fundamental and harmonics without additional processing, and the speed of operation. The claims are verified through extensive simulation studies in MATLAB[®]/Simulink[®].

Index Terms—Amplitude-locking, phase-locking, harmonics extraction, amplitude demodulation.

I. NOMENCLATURE

$x_I(t)$	Instantaneous value of amplitude modulated carrier-based input signal x_I .
$y(t)$	Instantaneous value of extracted carrier from x_I .
$d(t)$	Desired amplitude of the carrier output y .
$c(t)$	Instantaneous value of the modulating signal in x_I .
$u(t)$	Instantaneous value of reciprocal of $c(t)$.
$x_P(t)$	Instantaneous value of phase-locked loop (PLL) corresponding to the carrier.
$C_k(t)$	Instantaneous amplitude of k^{th} harmonic in x_I .
ω_o	Frequency of fundamental component in x_I .
$x_O(t)$	Instantaneous value of output signal.
$a_O(t)$	Instantaneous amplitude of the carrier in y .
$A_O(t)$	dc component in a_O .
$x_E(t)$	Instantaneous value of error signal.
$X_E(t)$	dc component in x_E .
B_P	Amplitude of PLL output.
ω_c	Cut-off frequency of low-pass filter.
G	Integrator gain.

II. INTRODUCTION

The extraction of harmonics or the fundamental components of voltages and/or currents is one of the main parts in the

implementation of custom power devices. The techniques available can be broadly classified into single-phase and three-phase. They can also be classified into open-loop techniques and closed-loop techniques. A comparative evaluation of some of these methods can be found in [1] and the importance and applications of proper extraction can be found in [2]. The closed-loop techniques have the distinct advantage of being capable to stay synchronised (zero-deviation, amplitude/phase-locked, to be more precise) to the input, which is very important in all applications connected to the grid. Extracting the fundamental/harmonics in a single-phase signal in a closed-loop scheme is the main focus of this paper. The proposed scheme falls into the class of closed-loop techniques presented in [3]–[7]. Phase and amplitude locking has been in use in the communication area for the purpose of amplitude modulation/demodulation. In the year 1991, a vector-locked loop (VLL) was presented by DaSilva in a patent [6] which uses peak detection in the magnitude detection stage. Pettigrew presented an amplitude-locked loop (ALL) in another patent [8] in the year 1994. Both the aforementioned schemes assume the input to be a sinusoid and hence can not directly be used for extracting harmonics from distorted inputs. Later Moir [3] has presented an analysis of the scheme by Pettigrew. Luo, et. al., [4] has the desirable feature of staying locked to the PLL reference and is very simple to understand and implement. However its settling-time is a function of the integrator gain and an increase in the gain to improve dynamic performance results in increased distortion in the filtered output. A VLL for synchronous extraction of harmonics was presented for the first time in 2002 by H. Karimi et. al., [7]. The performance is similar to that of the scheme presented by Luo, et. al., since it uses the same structure in the amplitude extraction section of the algorithm. An improved scheme was presented by M. Karimi-Ghartemani et. al., in [5] in 2003, where a low-pass filter is introduced in cascade with the integrator which improves the steady-state response and allows for a higher gain thereby reducing the settling-time.

In this paper the ALL given by Pettigrew is adapted for extraction of harmonics using its demodulation property. It's

unique feature is in identifying that the ALL can also do the job of fundamental extraction by extending the analysis provided by Mior [3], developing the mathematics to prove the idea, and suggesting modifications to improve the performance parameters. A flat second-order-low-pass filter(SOLF) pretuned to a cut-off frequency (ω_c) for smoothing the error in the fundamental extraction is used for improving the performance.

The paper is organised as follows: In Section III, a brief review of the analysis presented by Moir is presented in order to understand the operation and to make the context clear. The adaptation of the scheme to extract the fundamental is explained in Section IV with mathematical proof. The design parameters influencing the performance parameters are identified. Design considerations are discussed in Section V and empirical rules are developed for design. Simulation results are presented in Section VI.

III. BRIEF DESCRIPTION OF PETTIGREW'S ALL

The amplitude-locked loop (ALL) proposed by Pettigrew in the year 1994 in a patent [8], is shown in Fig.1 below. T. J.

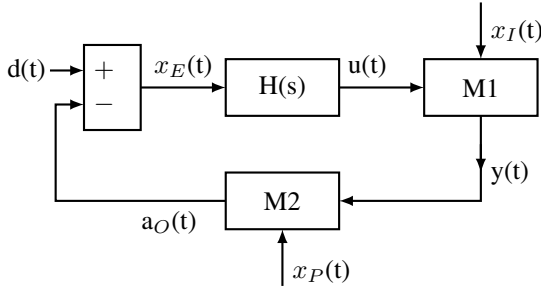


Fig. 1. Block diagram of Pettigrew's ALL

Moir [3] presented an analysis of the circuit. The idea used is captured in the following short description. In the circuit shown in Fig.1, the output of the multiplier-M1 is,

$$y(t) = u(t)x_I(t). \quad (1)$$

Consider an input,

$$x_I(t) = c(t) \cos(\omega_o t + \phi_i) \quad (2)$$

where $c(t)$ is the modulating signal and $\cos(\omega_o t + \phi_i)$ being the carrier. For the purpose of analysis $c(t)$ and ϕ_i are considered initially constants, but in practice may be time varying. It is assumed that $c(t) \neq 0$. The signal $x_P(t)$ is given by,

$$x_P(t) = B_P \cos(\omega_o t + \phi_p) \quad (3)$$

obtained as the output derived from a PLL tuned to the carrier frequency ω_o . Let the output of the multiplier-M2 be,

$$a_O(t) = x_P(t)y(t). \quad (4)$$

When the ALL is 'in lock' the error signal,

$$X_E(s) = D(s) - A_O(s) \quad (5)$$

$$= D(s) - X_P(s) * Y(s) \quad (6)$$

where $*$ denotes convolution. With the approximation of ignoring $2\omega_o$ terms in $x_E(t)$, and considering $H(s) = \frac{G}{s}$ and $B_P = 1$ it is shown in [3] that,

$$U(s) = \frac{G}{s + c \frac{G}{2} \cos(\phi_n - \phi_i)} D(s). \quad (7)$$

With step input of magnitude D for $d(t)$ and with $x_E(t)$ converging to zero in steady state, the response is,

$$u(t) = \frac{2D}{c \cos(\phi_n - \phi_i)}. \quad (8)$$

If $\phi_i = \phi_n$, which is usually the case, then,

$$u(t) = \frac{2D}{c} \quad (9)$$

i.e., $u(t)$ becomes the scaled inverse of the amplitude, c of the input $x_I(t)$. Then from (1) and (2),

$$y(t) = 2D \cos(\omega_o t + \phi_i) \quad (10)$$

which is a scaled version of the carrier $\cos(\omega_o t + \phi_i)$, where $2D$ is the scalar, as decided by the amplitude reference $d(t) = D$. Note that $y(t)$ is devoid of the modulating signal c , hence is amplitude demodulated version of $x_I(t)$. Equation (10) shows that the system has the ability to remove the modulating signal leaving only the carrier. Then $u(t)$ becomes the scaled inverse of the amplitude of the input. That is, the ALL tracks the inverse of the modulus of the input.

Although the analysis is only true for constant c , it is intuitive that for the time-varying case with the frequency and depth of modulation within the tracking range,

$$u(t) = \frac{2D}{c(t)} \quad (11)$$

and $y(t)$ is still given by (10).

IV. ADAPTATION OF PETTIGREW'S ALL FOR FUNDAMENTAL/ HARMONICS EXTRACTION

A. Basic operation

Consider a signal input $x_I(t)$, a periodic waveform with a dc component,

$$x_I(t) = x_{DC}(t) + \sum_{k=1}^{\infty} C_k \cos(k\omega_o t + \phi_k). \quad (12)$$

The output of the PLL (pretuned to a free-running frequency of ω_o) which is purely sinusoidal and in phase with the fundamental component of $x_I(t)$ is,

$$x_P(t) = \cos(\omega_o t + \phi_1) \quad (13)$$

where $B_P = 1$ is considered. Now each term in (12), can be considered as the product of a modulated signal determined by the coefficient C_k and a carrier determined by ω_k . If there was only fundamental at ω_o and with PLL tuned to ω_o , it is clear from (8) and (9) that C_1 can be obtained by the reciprocal of $u(t)$ and appropriately scaled due to the commanded amplitude D factor. It is also clear from (9) that D shall be chosen as 0.5.

It is also true that a_O , which is obtained as a multiplication of two in-phase sine waves of like frequency contains a dc, equal to half the product of each of the amplitudes. Hence in this scheme D shall be set as 0.5. It should be noted that a_O also contains $2\omega_o$ components, which is attenuated by the integrator in the $H(s)$. Additional attenuation can be achieved, as will be explained shortly. The product of C_1 and $x_P(t)$ recovers the input signal for this case of single frequency input. Thus,

$$x_O(t) = c(t)x_P(t). \quad (14)$$

It should be noted that, under the steady-state, the fundamental amplitude of $y(t)$ shall be unity, until then the corrections will continue.

B. Principle of working for input with dc and harmonics

It should be noted that any component in $x_I(t)$ other than ω_o , including dc, will not produce a dc in $a_O(t)$, according to (4). Thus it will not affect the transient response of $u(t)$ and hence $c(t)$, as it is decided by the rate of charging the integrator which is determined by the dc component in $x_E(t)$. So, all such terms in (12), will not affect the transient response. However they have a direct bearing on the steady-state response of $c(t)$, and show up as ripple in it. However the steady-state and transient performances can be improved by inserting a low-pass filter $F(s)$ as shown in Fig. 2.

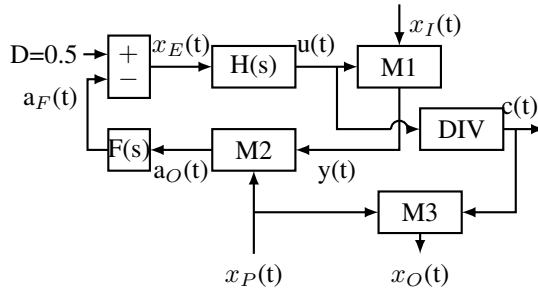


Fig. 2. Block diagram showing the adaptation

Ideally $F(s)$ should pass only the dc, blocking the fundamental (which may creep-in due to the presence of dc in x_I) and all higher order harmonics. Hence the cut-off frequency should be considerably less than ω_1 . Then there will be faster attenuation of the harmonics in the loop and the settling-time improves alongwith improvements in the other performance parameters.

V. DESIGN CONSIDERATIONS

It is to be noted that the design parameters are: gain G and, cut-off frequency ω_c and Q for the filter $F(s)$. And on the other side the performance parameters are: settling-time, harmonic rejection, amplitude modulation, and noise rejection. Extensive simulation study is done and experiments are conducted to arrive at a good set of values for the design parameters. It should also be noted that there is a need to limit the lower level for $u(t)$, atleast during the start-up. Otherwise division by zero can create problem and also the amplitude $c(t)$ of

the fundamental in x_O , will start building from unrealistically large values, making the settling time unnecessarily larger. This limit can be chosen with the knowledge of practical range of amplitude for the fundamental under the given circumstances.

A. PLL Design

This scheme works in association of a PLL. Note that the proposed ALL output will be of the same frequency as that output by the PLL. Therefore it is necessary to design the PLL with a free-running frequency close to the fundamental frequency component in the input. The PLL performance can be optimized by well established techniques.

B. Design of the circuit

The function of the low-pass filter is to attenuate the harmonics generated in $a_O(t)$ with the presence of higher order harmonics in $x_I(t)$ and as well as the second harmonic produced due to the interaction of the fundamanetal in $x_I(t)$ with $x_P(t)$. And it is also necessary that it does it as fast as possible. Hence it is found through experiment that a flat second- order-low-pass filter is a good choice and a suitable cut-off frequency of ω_c is selected. The transfer function of the low-pass filter is as given below:

$$F(s) = \frac{1}{\frac{s^2}{\omega_c^2} + \frac{s}{Q\omega_c} + 1} \quad (15)$$

where ω_c is the cut-off frequency in rad/s. It is observed while tuning that an increase in gain G (for a fixed ω_c), results in an increases in steady-state error and a decrease in settling time. A similar relation holds good for a change in ω_c (for a fixed G). This makes tuning of the algorithm very easy, however the relations are not linear.

VI. SIMULATION RESULTS

Extensive simulation studies were conducted on this scheme using MATLAB® and Simulink®. A simulation step-size of $10\mu s$ is chosen. Various features of the system with $\omega_c = 70\pi$ rad/s, $Q = 0.85$, and $G = 118$ were explored for different inputs. A lower limit of 0.2 for u ($\equiv 5$ for C_1) was set. The results are presented in what follows.

A. Response to Step Input: The amplitude C_1

A square wave input of unit amplitude with a frequency of $\omega_o = 100\pi$ rad/s, is applied to the circuit at $t = 0.1$ s. The settling-time indicated by the signals u and c is captured in the Fig. 3. It can be observed that the system settles to final value within around 1.5 cycles, which much better than the existing schemes.

B. Response to Step Input: The fundamental $x_1(t)$

The input square wave and the fundamental extracted signals are as shown in Fig. 4. The expected fundamental amplitude ($\pm \frac{4}{\pi}$) is also plotted to show the settling-time. It can be clearly seen that the fundamental settles within 1.5 cycles.

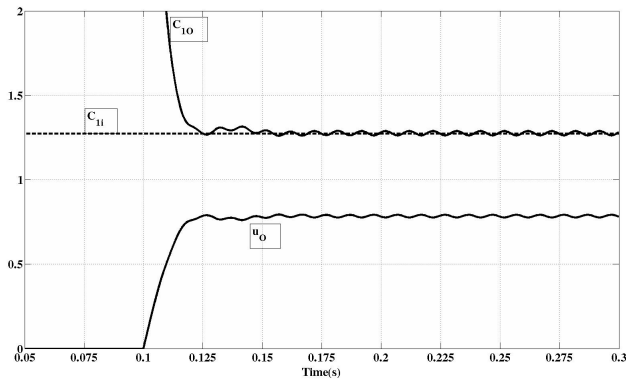


Fig. 3. Step response showing settling time for a square wave input

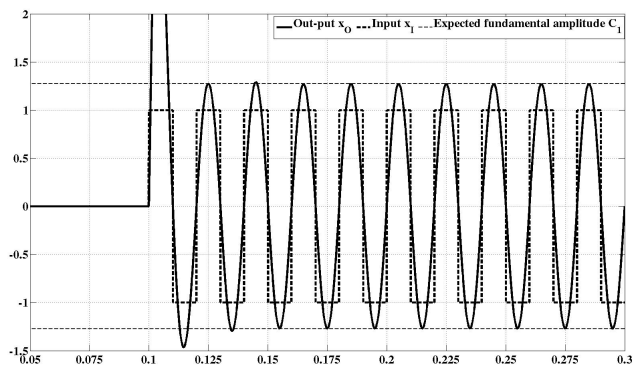


Fig. 4. Out-put for a square wave input

C. Response to Step Input: The Harmonics in $x_I(t)$

The harmonics extracted from the square wave is shown in Fig. 5.

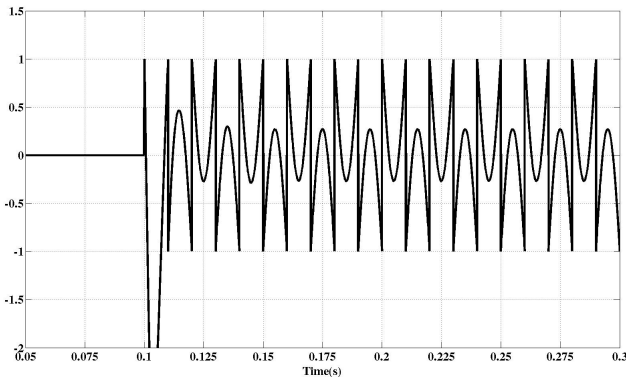


Fig. 5. Harmonics extracted from a square wave input

D. Response to Input Amplitude Modulation

The performance of the scheme is verified for tracking a slow varying amplitude, as might happen in power system. This feature is also important for amplitude demodulation. The input considered is:

$$x_I(t) = [1 + 0.2 \sin(4\pi t)] \sin(100\pi t). \quad (16)$$

Fig. 6 displays an area zoomed to around one cycle of the modulating signal in order to clearly show the negligible phase lag in input modulating signal and the output.

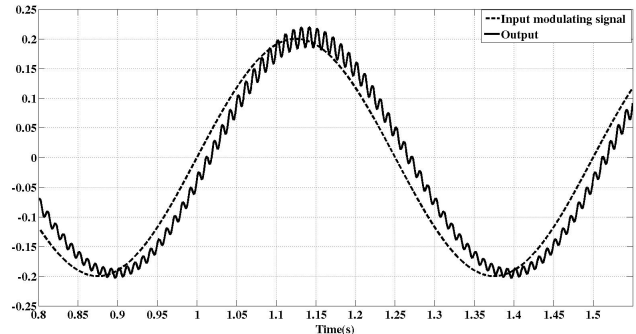


Fig. 6. Output amplitude to an input whose amplitude is modulated

VII. CONCLUSIONS

A scheme for obtaining synchronized selective-frequency amplitude-locking on distorted signals is presented, by adapting the Pettigrew's ALL. An intuitive explanation of the working of the loop is presented. Clear explanations are given for the selection of G and Q . Performance claims are supported by simulation results. The features of the proposed scheme are as follows: it has features similar to a PLL, the performance can be optimized by appropriate choice of G , ω_c , and Q , the transient response is better ($\cong 1.5$ cycles), has excellent insensitivity to harmonics, and noise rejection. It can find applications in: synchronous separation of the fundamental and harmonics in a distorted periodic waveform, amplitude and frequency tracking, noise rejection, and amplitude demodulation/peak detection.

As a scope for future work a complete and rigorous mathematical analysis of the proposed scheme can be in order.

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